

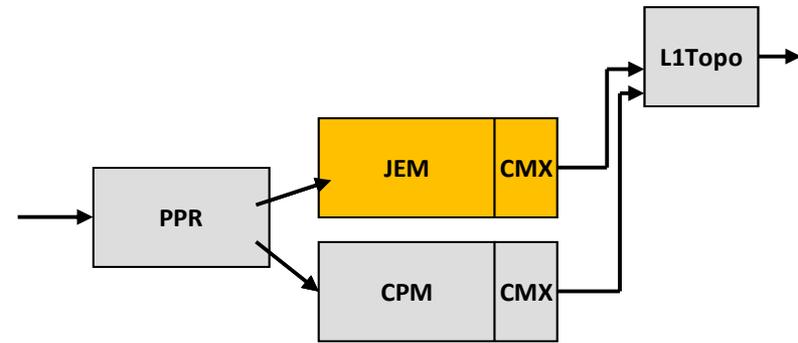
jFEX

Mainz

Jet processing

Phase-0 jet system consisting of

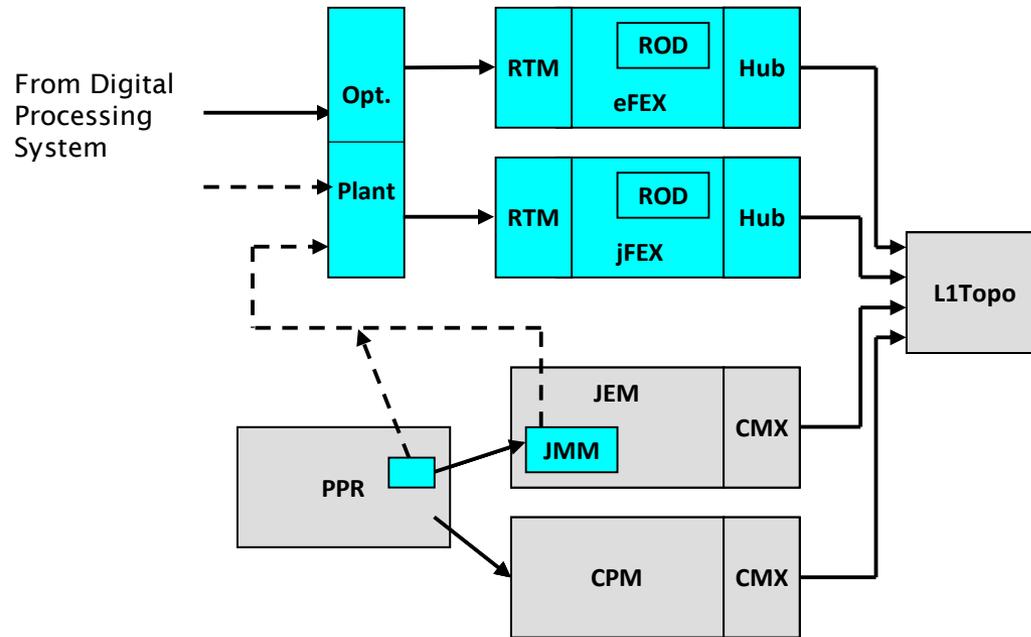
- Pre-Processor
 - Analogue signal conditioning
 - Digitization
 - Digital signal processing
 - Jet element pre-summation to 0.2×0.2 ($\eta \times \phi$)
- Jet processor
 - Sliding window processor for jet finding
 - Jet multiplicity determination
 - Jet feature extraction into L1Topo (pre-phase1)



At phase-1: complement with jet feature extractor jFEX

- Improve on jet finding (and MET measurement)
- LAr signals optically from digital processor system
- TileCal signals three options

L1Calo Phase-1 System



 New at Phase 1

jFEX input data

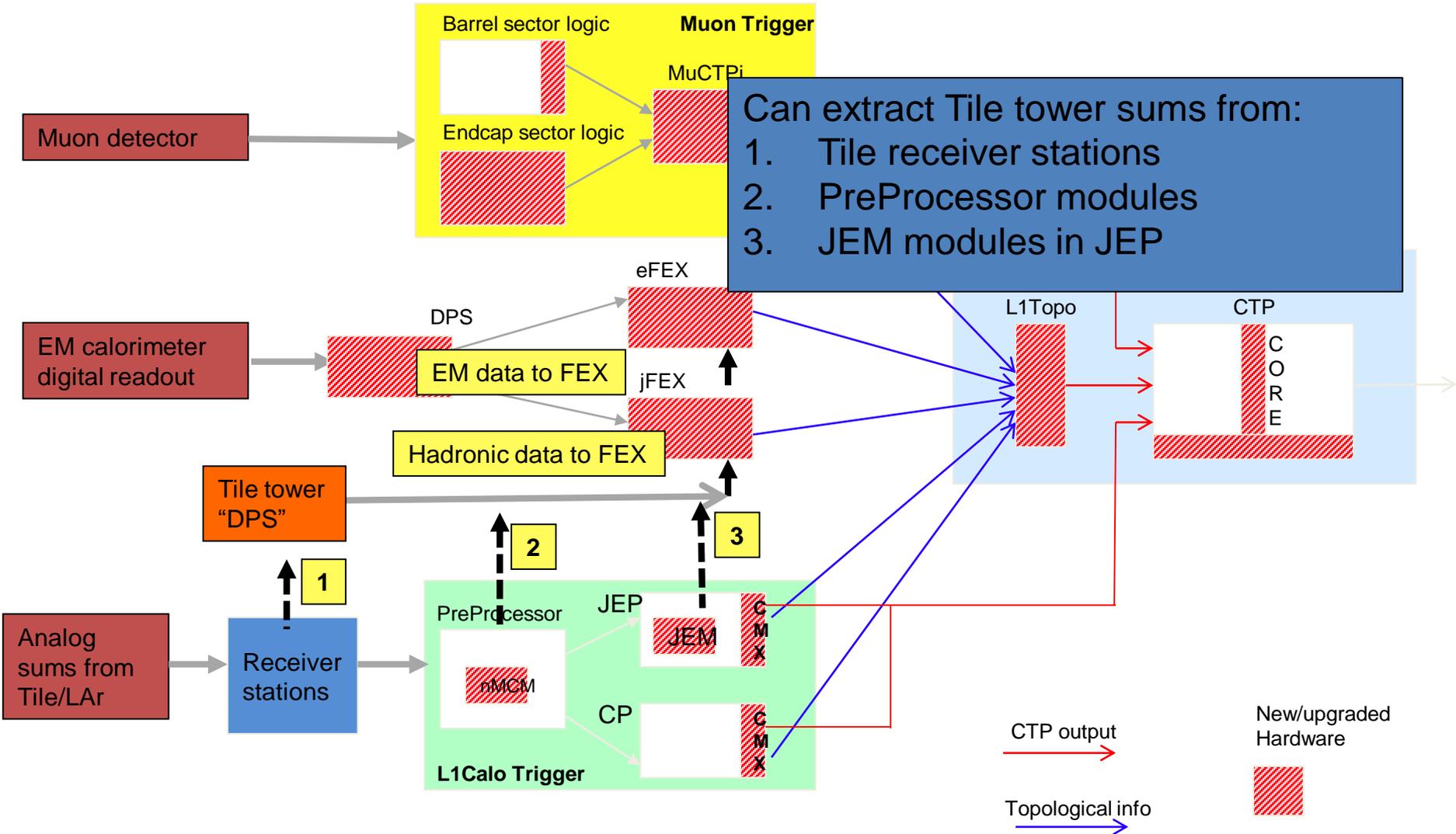
- Fibre optical inputs only
- Fibre bundles via patch panel / fibre re-bundling stage
- Granularity $.1 \times .1$ ($\eta \times \varphi$)
- One electromagnetic, one hadronic tower per $\eta \times \varphi$ bin
- Unlike eFEX, no "BCMUX" scheme possible due to consecutive non-zero data
- 6.4 Gb/s line rate, 8b/10b encoding, \rightarrow 128 bit per BC
- 16bit energy per tower, 8 towers per fibre
- LAr data from DPS
- Tile ...

FEX input data – TileCal

Three options for getting TileCal data onto opto fibres

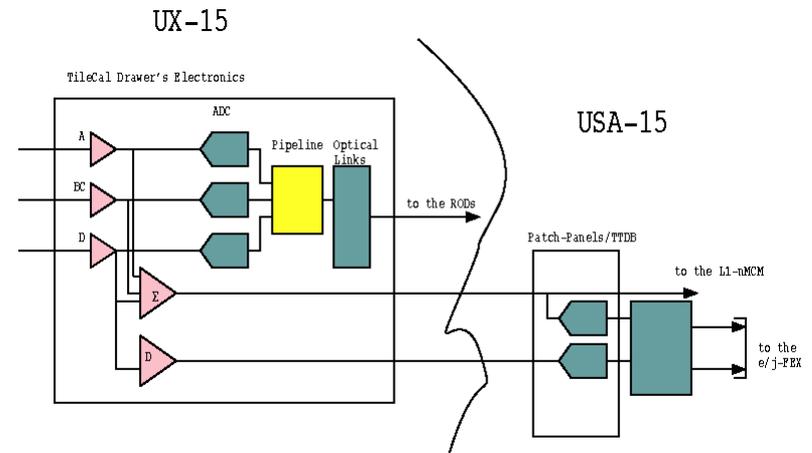
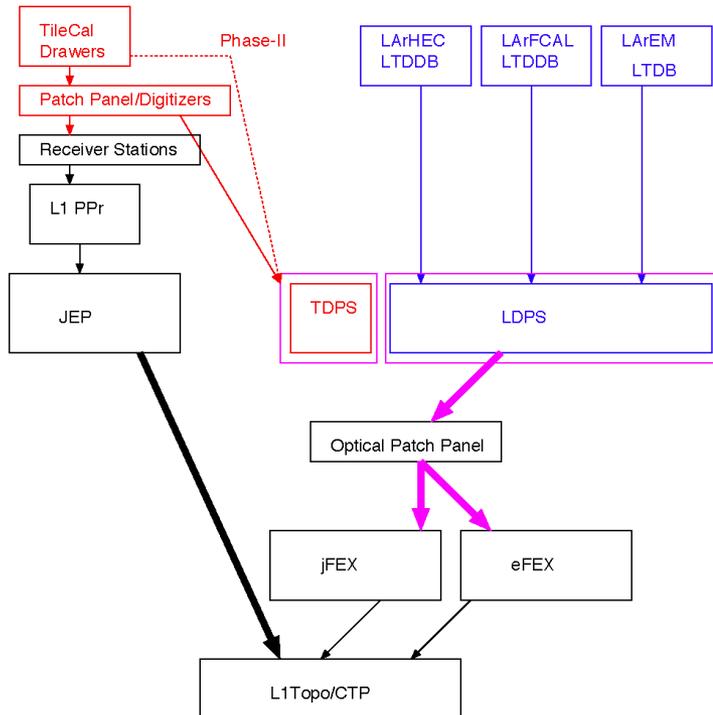
- Option 1 – replicate analogue TileCal trigger signals into additional TileCal digitizer stations
- Replicate existent L1Calo digital electrical output into fibres
 - Option 2 : At source (Pre-Processor)
 - Option 3 : At sink (Jet/Energy Processor)

TileCal input options



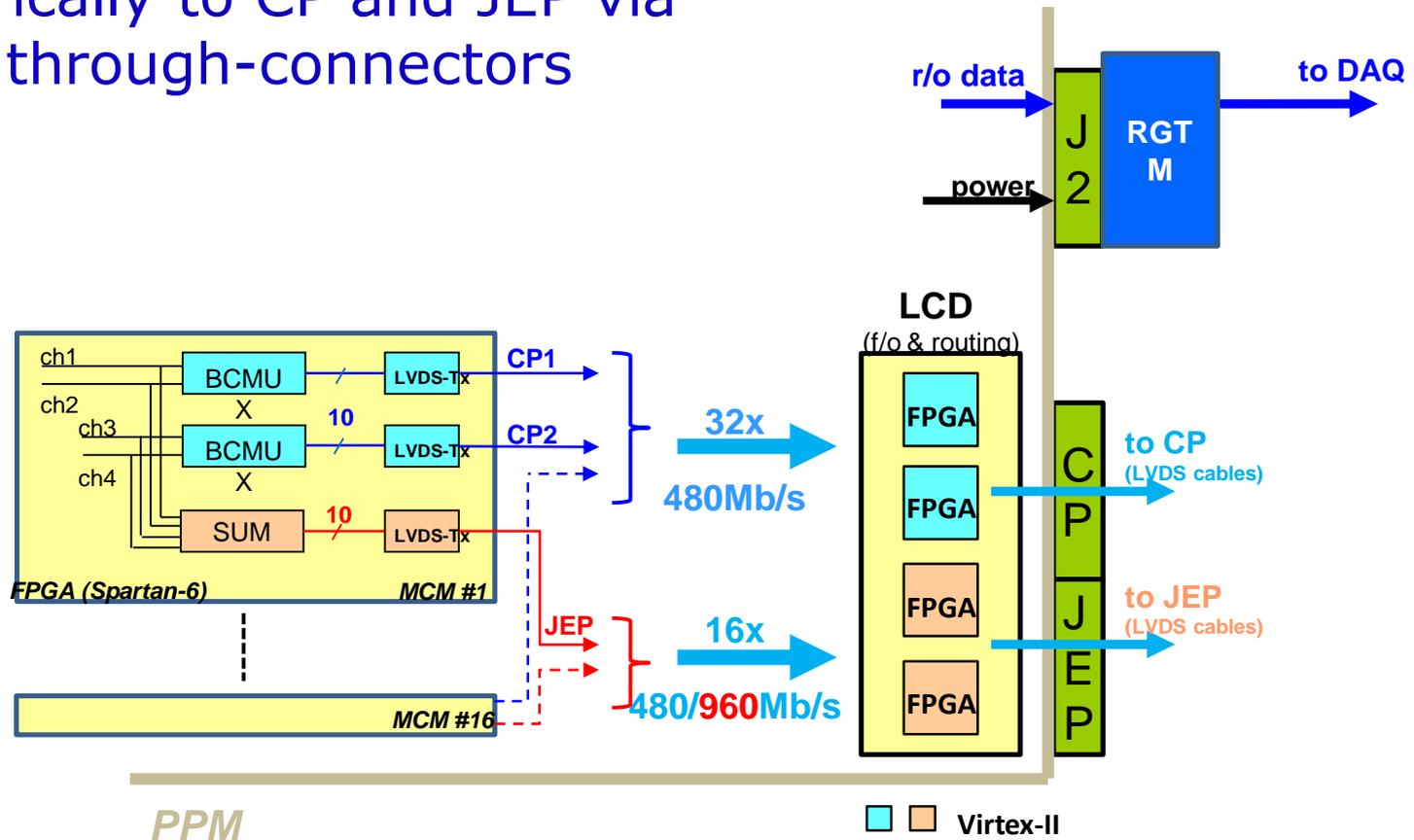
Option 1: Tile stations

- Signals extracted at arrival point in USA15
- Build a new system to digitize and process analog signals
 - Patch panel / split off analog signal to be digitized
 - Digitizer
 - Serializer / fibre driver
 - TDPS (incl. L1 PP)



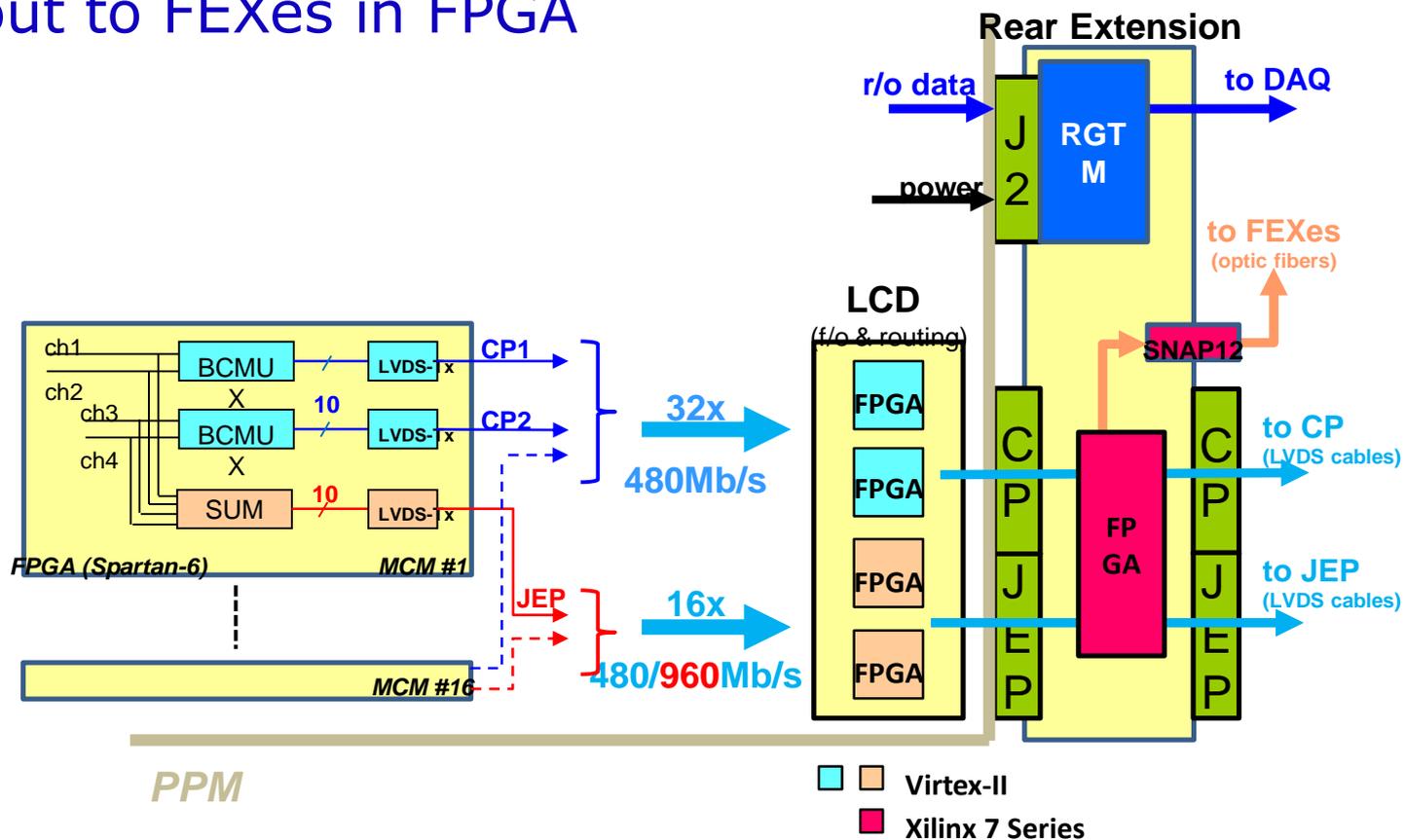
Pre-phase1 Pre-Processor System

- nMCM with firmware option to serialize to 960Mb/s
- Phase0 LCD card
- Data electrically to CP and JEP via backplane through-connectors



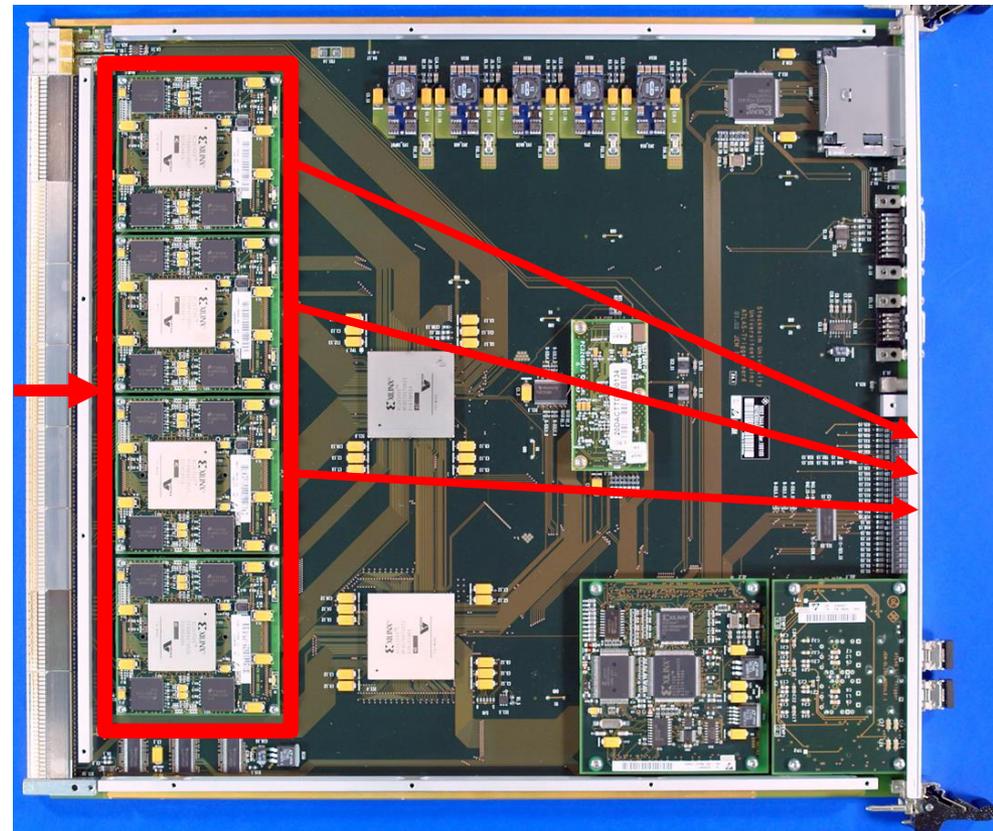
Option 2, PPM h/w upgrade

- Add rear transition module
- Equip with FPGA (V7) and 12-channel e/o transmitters
- 4-fold fan-out to FEXEs in FPGA



Option 3: JEM h/w Upgrade

- New input daughter card (JEM Mezzanine Module) at phase-1
- Virtex-7 based
- Receive 960Mb/s (i.e. double rate) high granularity tile data electrically
- Loop through to MGTs w/o processing
- Run through MicroPOD transmitters
- 4 copies of incoming data to FEXes via front panel



Considerations

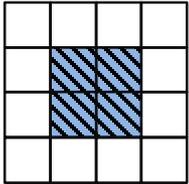
Need to assess:

- Latency
 - Latency figures for O1 not known
 - Minor differences O2 / O3 (signal path)
- Dynamic range / resolution (would like to improve...)
 - Current L1Calo towers have 8 bit dynamic range with 1GeV/LSB
 - O2/O3 limited by ENOB of ADCs or noise *"equivalent number of bits"*
 - O1 limited by analogue noise (can we get any better?)
- Cost to implement
 - O2 and O3 using existent digitization and pre-processing
 - O3 basically just adding optoelectronics to a module that we are prepared to replace anyway, plus new LCD on Pre-Processor
 - O2 similar in terms of FPGA needs and optoelectronics
 - O1 difficult (for me) to judge. A lot of all-new circuitry
- Risk of disruption to / interference with existing system
- Maintenance
- ...
- N.b. input geometry of FEXes (eta vs. phi strip) hasn't yet been finalized. Might affect cost/complexity for given option.

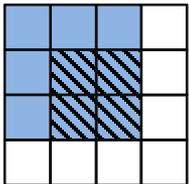
... and review, to narrow down options ... to 1 ...

Algorithms, now...

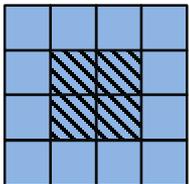
Sliding window algorithm (sliding in ϕ, η)



Operate on jet elements (towers) 0.2×0.2



Find and disambiguate ROIs sized 0.4×0.4



Calculate jet energy in three differently sized windows (programmable), up to 0.8×0.8

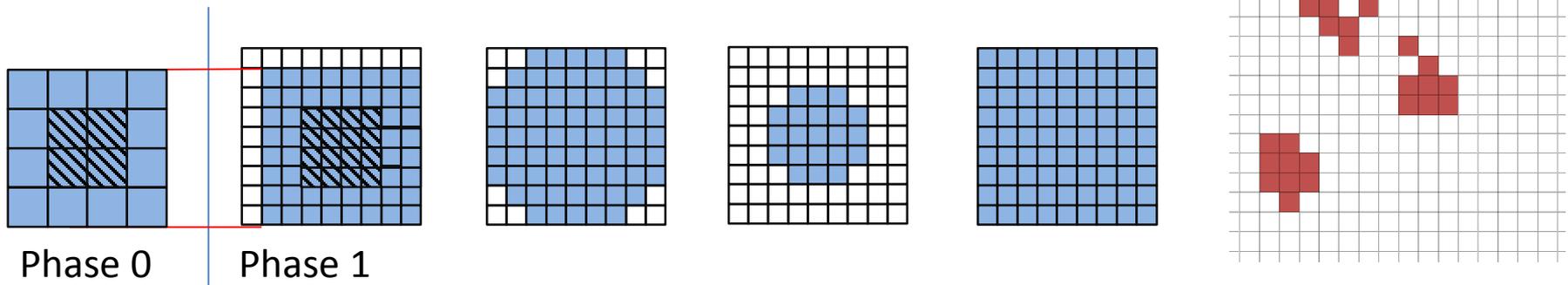


Jet size (window size) limited by environment (data duplication)

Granularity defined by arithmetic on Pre-Processor ASIC (pre-sum)

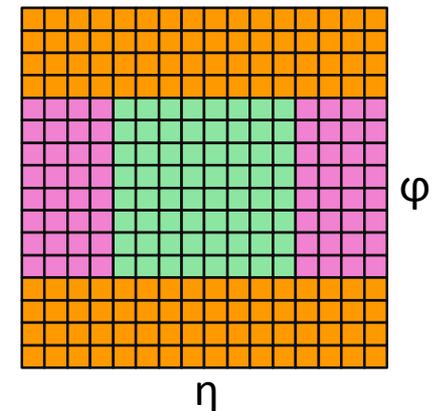
... and then

- Increase dynamic range
- Improve granularity by factor of four, to 0.1×0.1 ($\eta \times \phi$)
- Slightly increase environment (0.9×0.9 baseline)
- Allow for flexibility in jet definition (non-square jet shape, Gaussian filter, ...)
- Fat jets to be calculated from high granularity small jets
- Optionally increase jet environment



Data replication

- Sliding window algorithm requiring large scale replication of data
- Forward duplication only (fan-out), no re-transmission
 - Baseline: no replication of any source into more than two sinks
 - **Fan-out in eta** handled at source only (DPS)
 - Transmit **“core”** and **“environment”** data
 - Duplication at the parallel end (on-FPGA), using additional Multi-Gigabit Transceivers
 - Allowing for differently composed streams
 - Minimizing latency
 - **Fan-out in phi** handled at destination only
 - Baseline “far end PMA loopback”
 - Looking into details and alternatives
 - N.B. phi strip vs. eta strip organisation tbd.



jFEX partitioning

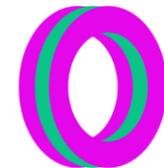
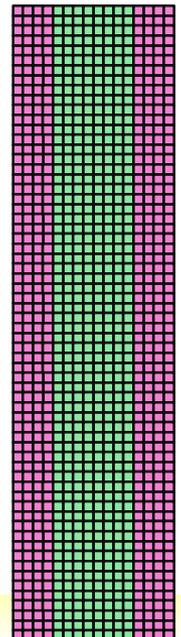
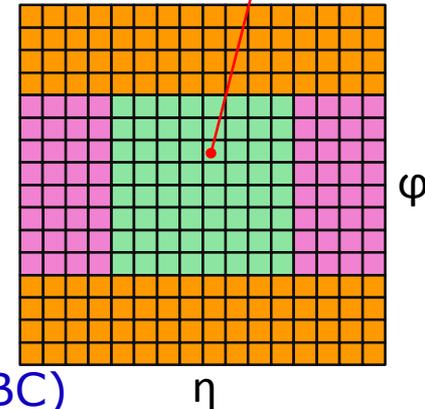
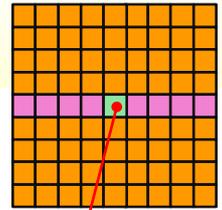
Algorithm requiring environment of 0.9×0.9 around each tower to be processed $\blacksquare \rightarrow \pm 4$ neighbours in eta and phi

Processor FPGAs

- **core of 0.8×0.8**
- Fully duplicated data in both eta and phi
- Total of 1.6×1.6 worth of data required
- 256 bins @ 0.1×0.1 granularity
- separate e/m + had channels \rightarrow 512 numbers (16-bit energies)
- That equals 64 on-chip receivers @6.4Gb/s (128 bit/lane/BC)
- Due to 100% on-board duplication, 32 of them are driven from a fibre

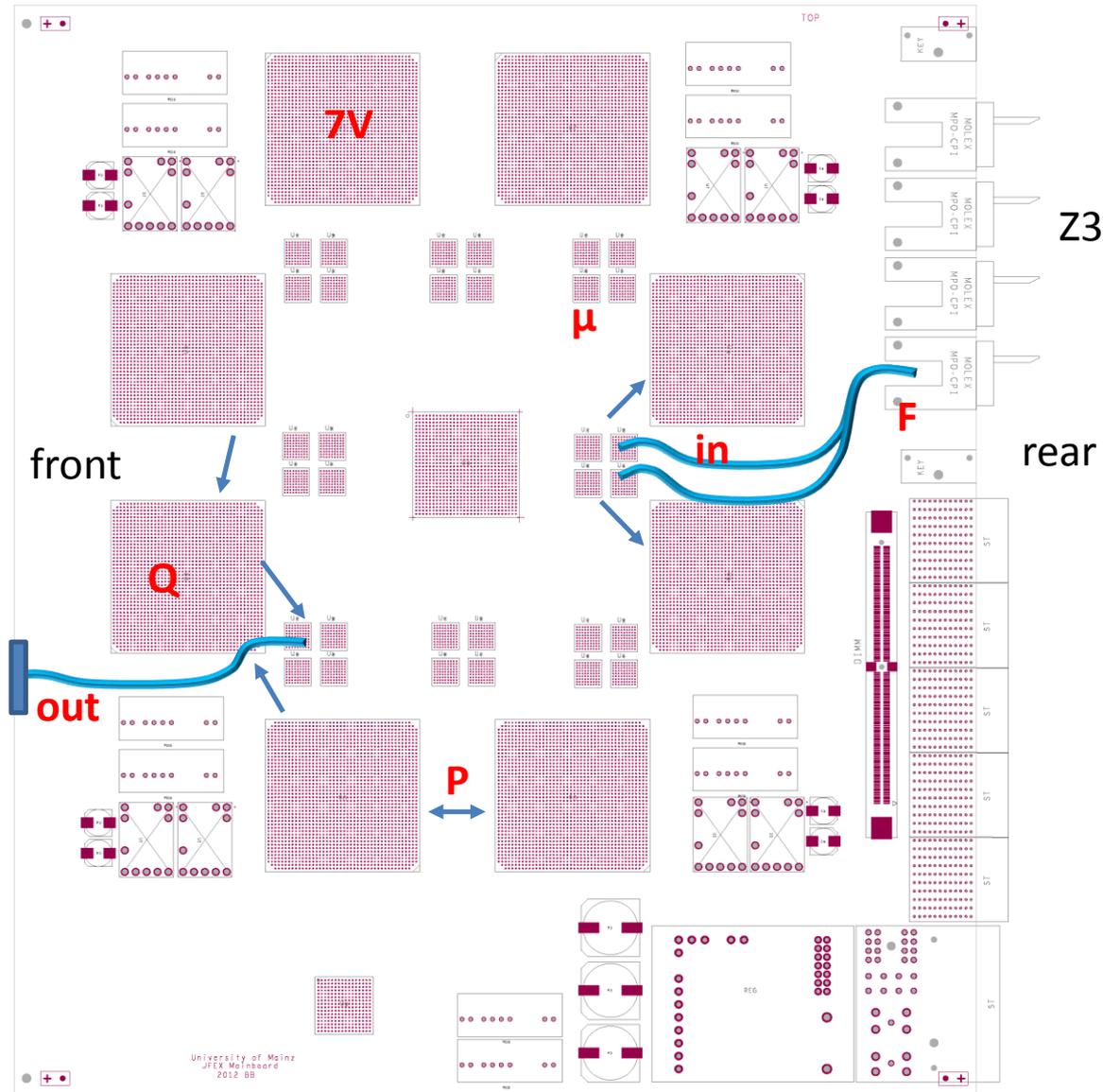
Processor modules

- Processing strip along phi
- Receiving fully duplicated data in eta from DPS
- Module covering full phi (8×0.8), limited eta range of .8
- Carrying 8 FPGAs
- \rightarrow total of $8 \times 32 = 256$ fibres coming in
- 22×12 -way opto modules "**MicroPOD**" high density receivers
- Four 72-way fibre connectors ("MPO/MTP")



How to fit on a module ?

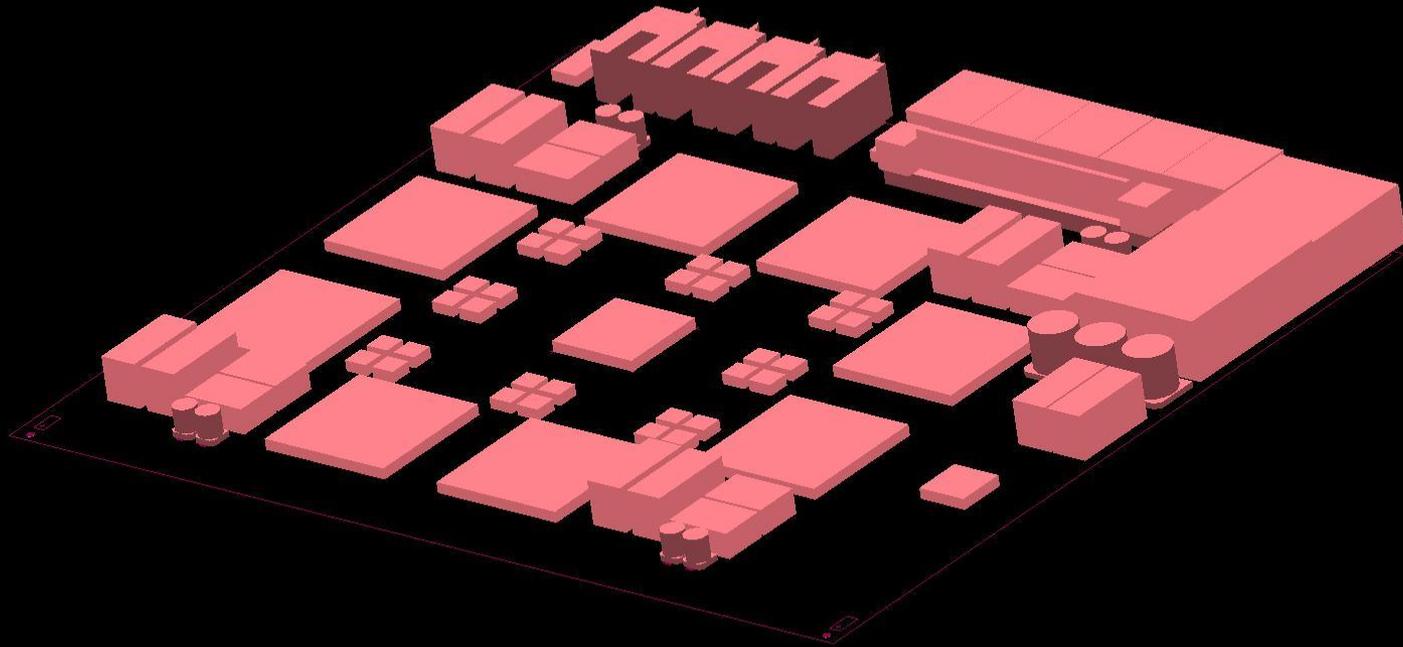
- AdvancedTCA format
- 8 processors (~XC7VX690T)
- 4 microPOD sockets each μ (including spare output)
- Opto connectors in Zone 3
- Fibre bundles from rear **F**
- fan-out via "far end PMA loopback" **P**
- consolidation of results on one of the processors **Q** (alternatively direct output)
- Output to front panel
- Small amount of module control logic / non-realtime (ROD)
- Maximise module payload with help of small-footprint ATCA power brick and tiny IPMC mini-DIMM



Z3

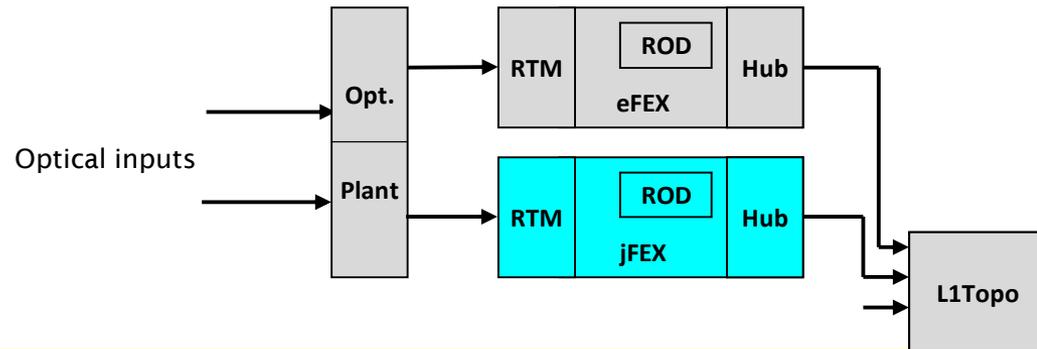
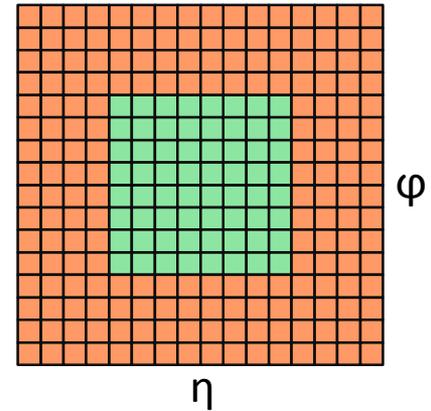
rear

...and 3-d



jFEX system

- Need to handle both fine granularity and large jet environment (minimum 0.9×0.9)
 - Require high density / high bandwidth to keep input replication factor at acceptable level (3/4 of all FPGA inputs are duplicates)
 - Fit in ~ 8 modules (+FCAL ?)
 - Single crate
- go for ATCA shelf / blades:
- Sharing infrastructure with eFEX
 - Handling / splitting of fibre bundles
 - ROD design
 - Hub design
 - RTM



Some considerations...

- jFEX relies on “MicroPOD” high-density optical devices
 - Electro-optical engine identical to popular “MiniPOD”s
 - Currently looking into mechanical and thermal issues
 - In contact to manufacturer to benefit from recent developments there
 - MicroPODs small enough to provide additional direct output from each processor FPGA if required (for fat jet determination on L1Topo module)
- 6.4 Gb/s baseline seems rock solid
- Fibre and module density are high but feasible
- Aim at higher line rates (currently FPGAs support 13 Gb/s, MicroPOD 10 Gb/s)
 - Allow for even finer granularity / larger jets / smaller FPGA devices :
 - If digital processor baseline allows for full duplication of 6.4Gb/s signals, the spare capacity, when run at higher rate, can be used to achieve a replication of more than 2-fold, so as to support a larger jet environment.
- The jFEX shall be compatible to phase 2
 - might affect organisation of input links (eta strips vs. phi strips)
 - Organisation of input links to be sorted out anyway

Firmware / Software

jFEX firmware

- Sliding window algorithm / feature extraction
- Board-level merging
- Monitoring and diagnostics
- Infrastructure for high speed links
- Module control
- DAQ (buffers and embedded ROD functionality)
- ATCA control
- TTC interface

Most items are common effort with eFEX

TileCal input – Example : JEM based TileCal inputs

- Serialization nMCM 960Mb/s
- Serialization JMM 6.4Gb/s
- Re-target existing JEM input firmware to new FPGA

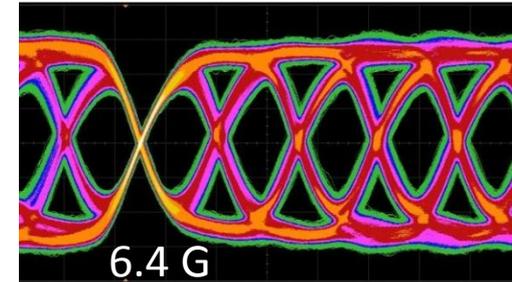
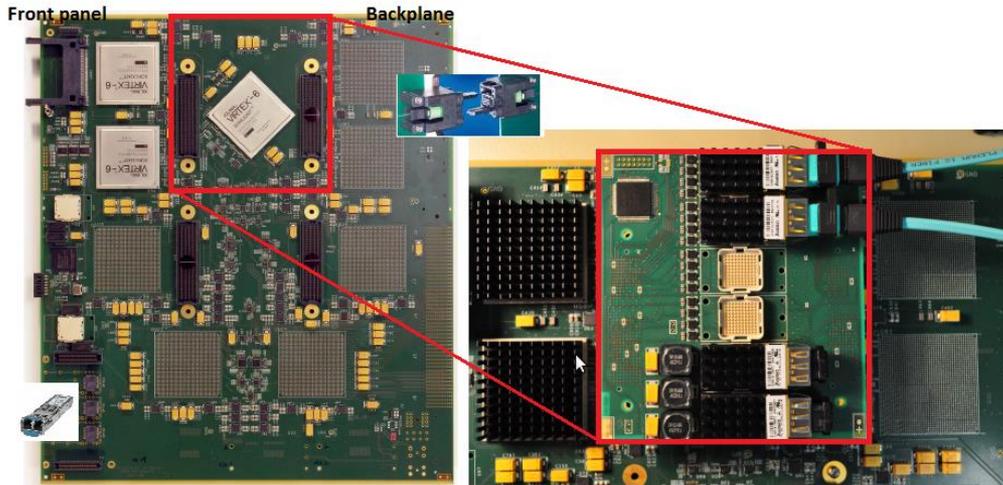
Software:

jFEX specific software is mainly register model and simulation of real-time path

jFEX development line at Mainz

- The jFEX is a further, advanced module within an ongoing development programme for high-speed opto-electrical, high performance processors
- Backplane & Link tester 2010
- Technology demonstrator "GOLD" 2011
- Level-1 Topology processor: Prototype to go into production early February 2013
- Test modules for specific aspects of data transmission
- MicroPOD test modules to be built and evaluated soon

Generic Opto Link Demonstrator – GOLD

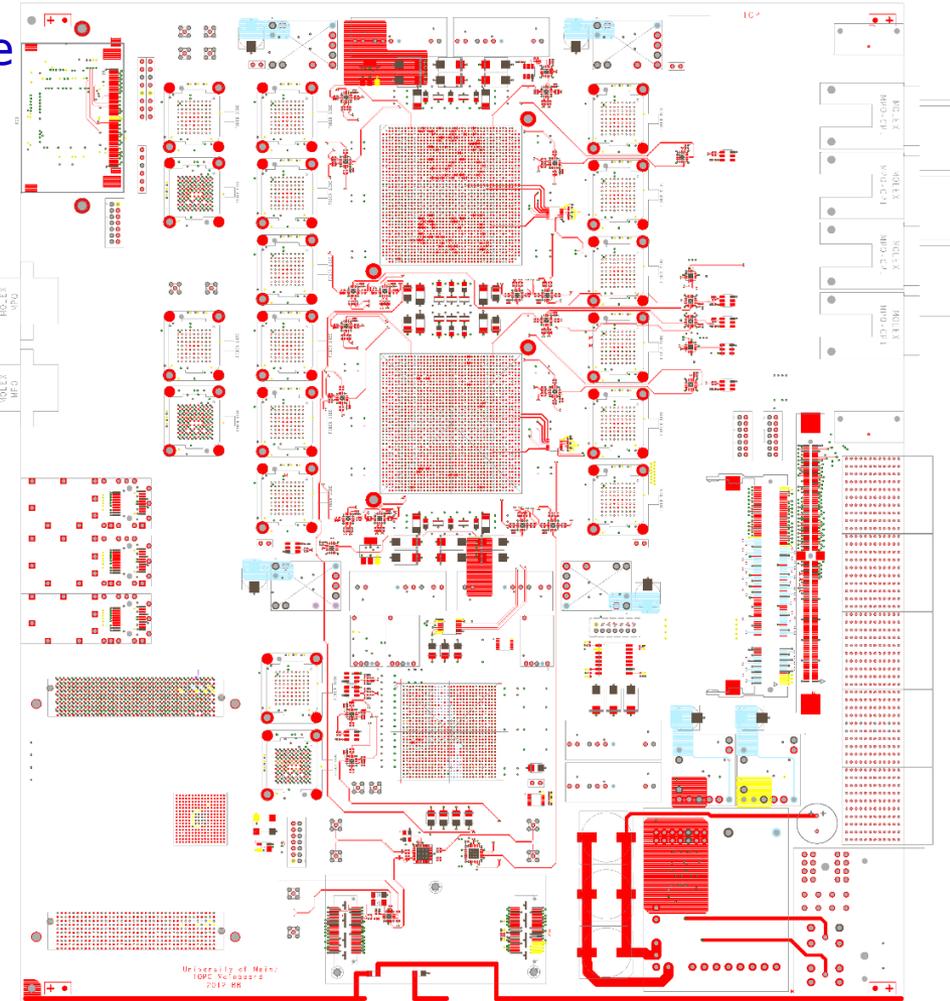


- Industry standard o/e converters (similar SNAP12) on mezzanine
- Designed for data paths up to 10Gb/s
- Including CML level fan-out devices
- Fibre input from the backplane (MTP-CPI connectors)
- Populated with mid range FPGAs (XC6VLX240T) up to 6.4Gb/s
- Successfully tested with TTC clock / jitter cleaner
- BER < 10^{-16}
- Continues to be used as source/sink for test bench

Topology processor L1Topo

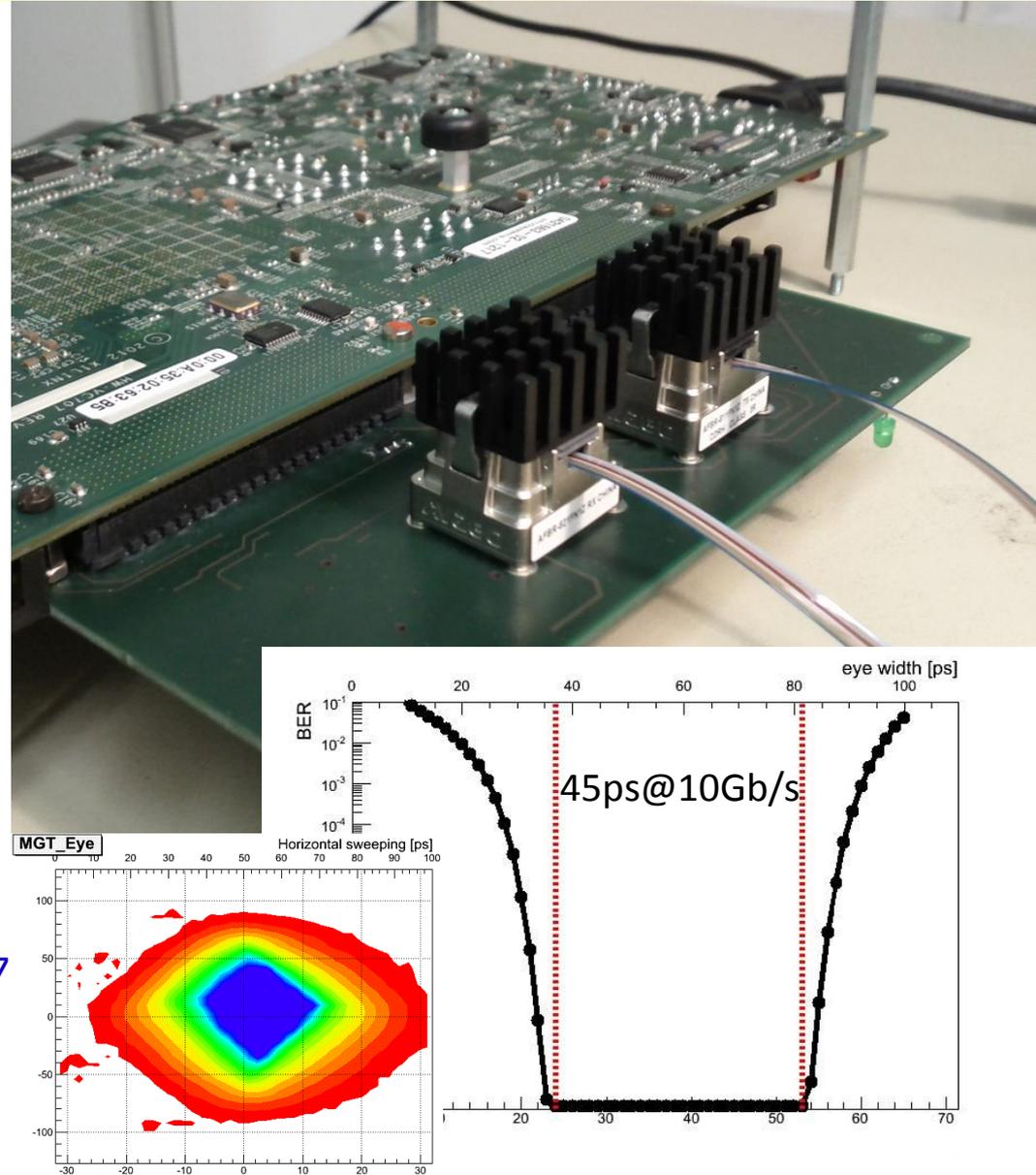
Same technologies as proposed for jFEX

- AdvancedTCA
- Real-time path:
 - Four 48-way fibre connectors zone 3
 - 14 fibre-optical 12-way inputs (MiniPOD)
 - Two processors XC7VX690T, 80 × 13Gb/s each
 - LVDS and optical output (front panel)
- Complex multi-rate clocking scheme LHC clock + crystals
- Several module control options (incl. Ethernet / IPbus etc.)
- Multiple processor FPGA configuration schemes
- Multiple options for DAQ and ROI interface
 - L1Calo style (SFP)
 - Embedded ROD / S-Link interface via MiniPOD

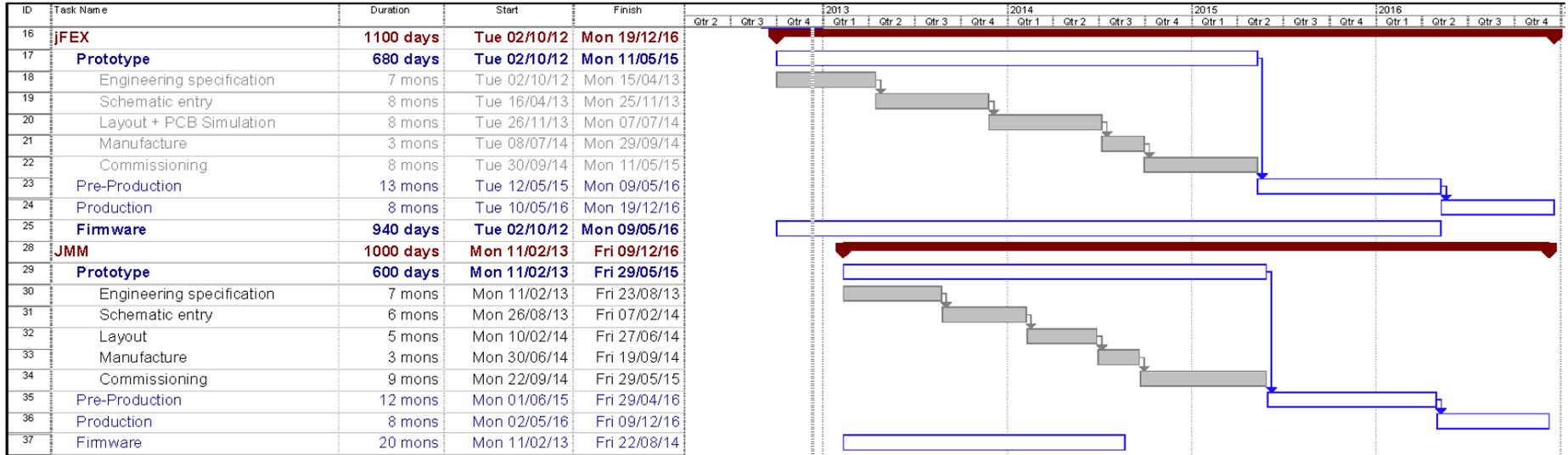


Minipod BER tests

- MiniPOD pair RX/TX on Xilinx XC7VX485T
- Loopback via 10m fibre bundle
- 3 stages of MTP/MPO connectors
- 6 channels exercised @ 10Gb/s
- No errors observed
- Bit error rate $< 6.4 \cdot 10^{-17}$



Schedule / Effort



Plus installation/commissioning/system tests thereafter.

Milestones: jFEX PDR Q2/2013
 FDR Q2/2015
 PRR Q2/2016

JMM PDR Q3/2013 - PRR Q2/2016

Also: resolution of Tile options and final designs before TDR

Effort

Requirements

- jFEX hardware, firmware: total of 17 FTE over 6 years, rather evenly spread until production...
- JMM mezzanine renewal (h/w+f/w) including TileCal fibre interface: total of 5 FTE over 6 years
- Integration, installation, commissioning (jFEX share): 6 FTE / 6 years

Known available effort:

Mainz is able to cover all required work on hardware, firmware and installation/commissioning of jFEX and JMM.

Total effort available: Physicist 5FTE, Engineer 1FTE per year

Heidelberg

is able to cover estimated need of 2 FTE/year on LCD and RTM

Total effort available > 2FTE/year

Conclusion

- The 8-module jFEX seems possible with ~2013's technology
- Key technologies explored already (GOLD, L1Topo,...)
- Use of MicroPODs challenging for thermal and mechanical reasons, but o/e engine is the same as in popular MiniPODs
- Scheme allows for both fine granularity and large environment at 6.4Gb/s line rate and a limit of 100% duplication of input channels
- Rather dense circuitry, but comparable to recent projects
- Even finer granularity and / or larger jets possible at higher transmission rates
- DPS needs to handle the required duplication (in eta)

Details of fibre organization and content cannot be presented now

→ Started work on detailed specifications, in parallel exploring higher data rates...

- TileCal signals required in FEXes in fibre-optical format
- Three options for generating them
- All seem viable, but probably at different cost. Need to converge.