JEM firmware

Uli

PRISMA

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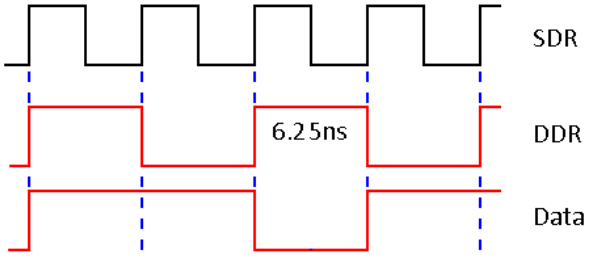
JG|U

Backplane data transmission

… following discussions at CMX review…

- Multiplex jet and energy sum data four-fold, to 160 Mb/s
- 24 source terminated data lines per JEM slot
- Data contents have been specified elsewhere
- Run a DDR clock signal (i.e. 80MHz) along the data lines
  - Source and sink terminated (on-chip)
  - Discussion on edge alignment between clock and data
  - CMXers will explore use of clocks edges lined up with data transitions at source
  - Possibly sub-optimal data window



… post CMX review…

→ started to look into JEM FPGA resources again

- Might be able to shift DDR clock edge to centre of data eye
- Check Virtex-2 resources – phase shifted clock vs. 160MHz …
  … just started (ISE 10.1 installed on Windows 8 …)

JEP firmware modification

- Real-time path on both jet and energy sum processor
- ROI data serialization to Level-2 on jet processor
- DAQ data collected and formatted on energy sum processor
  - Data stream from input modules unchanged
  - Parallel data path from jet processor cut down from 24bit to 8bit wide (presence map)
  - Energy sum fields to be extended
- Playback and spy memories on the merger data ports should probably be adapted, though they've never been used after initial test bench operation at Mainz (requires online software modifications as well!)

Only urgent activity is verification of phase shifted DDR clock option !

…two slides from Stockholm to follow…

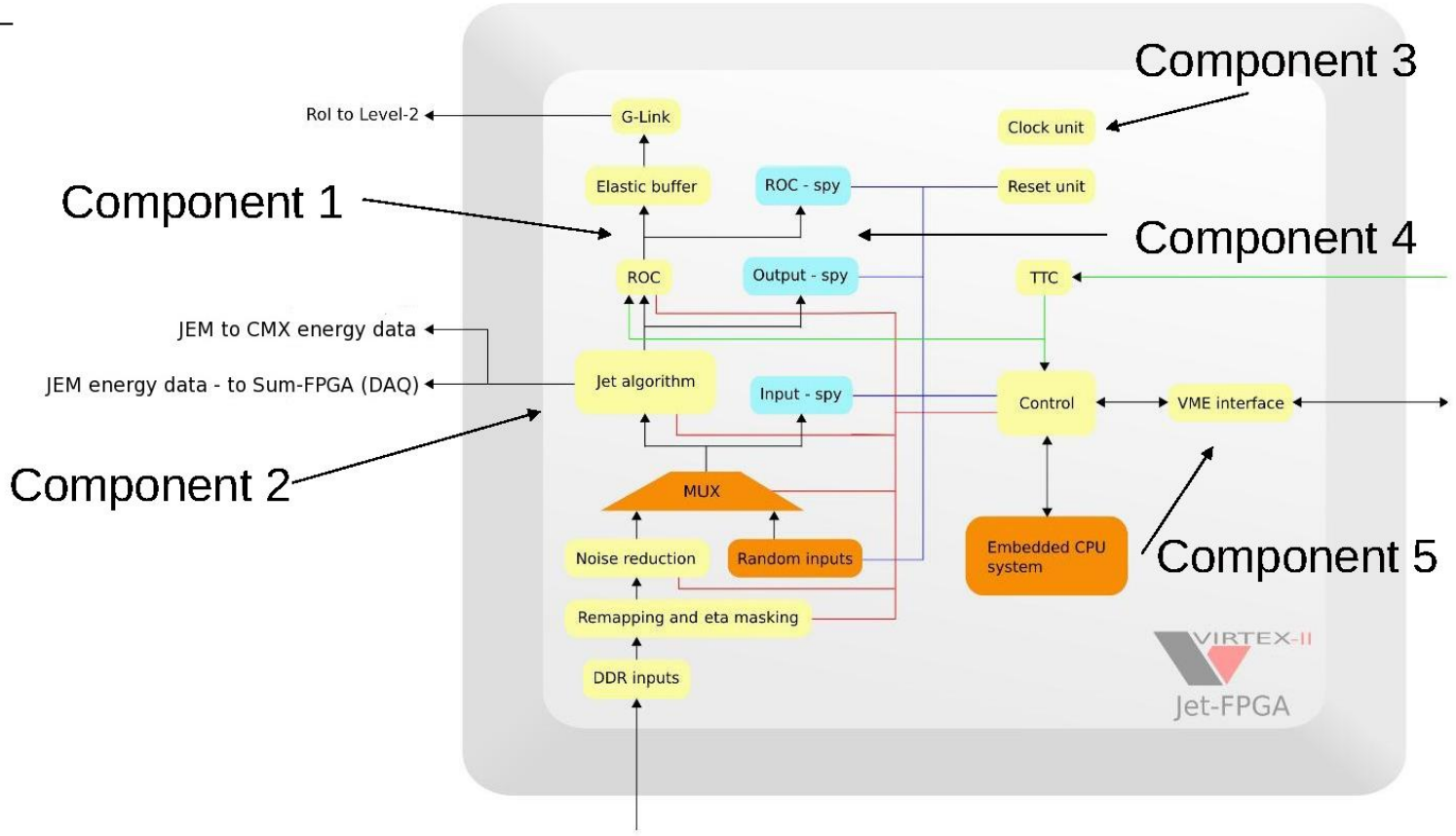
Jet processor

General remarks

- JEM firmware upgrade to add RoIs to the real time output.
- Algorithm will report up to four RoIs.
- No side effects. The latency will not be affected.
- 16 registers (thresholds) in use (in total 116 including spare).
- Updated components: Algorithm (including backplane and DAQ data), VME interface, Glink stream (RoI-to-L2), SPY Memory, Clock manager (DCM, 160MHz).
- No design overhauls and no FPGA resource limitations to implement new functionality.
- Verification method to approve a new firmware:
  Two methods in the lab (testbench and embedded system), while third one will be performed at CERN (JEM board with online software).

Jet processor

Architecture of the jet-FPGA



Architecture is modular, its easier to add, replace or modify...