jFEX

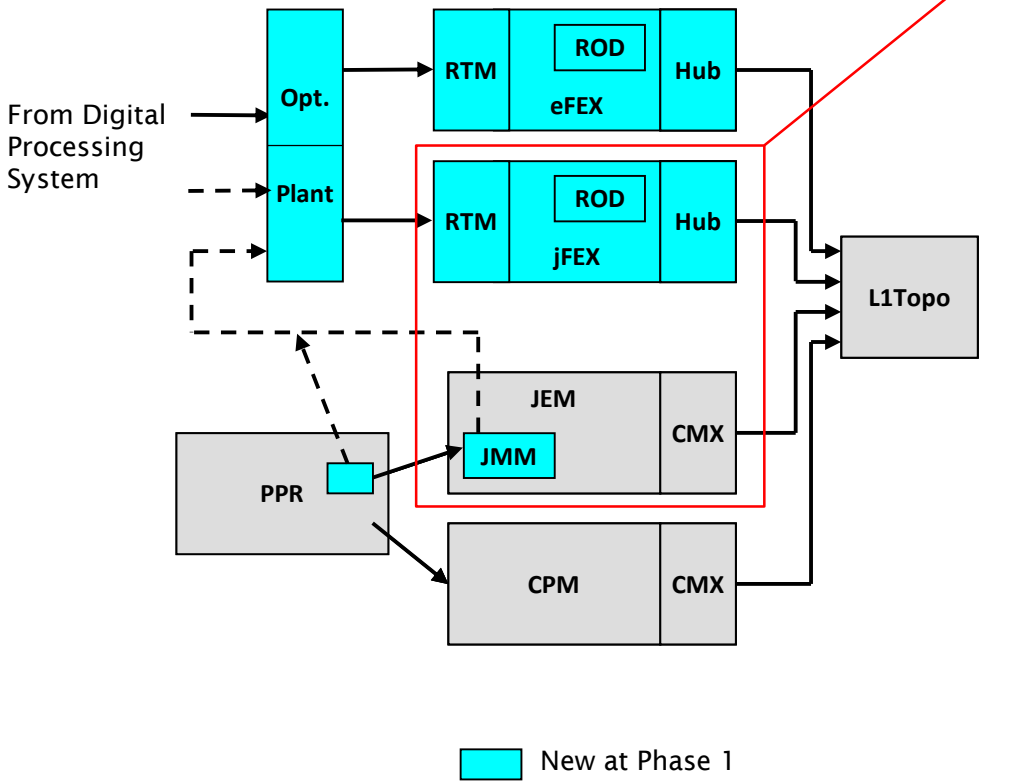
Uli

PRISMA

JOHANNES GUTENBERG UNIVERSITÄT MAINZ

JG|U

L1Calo Phase-1 System / Jets



Jets

Phase-0

- Jet elements 0.2 x 0.2 (η×φ) (pre-processor)
- Sliding window processor for jet finding JEM
- Jet multiplicity determination
- Jet feature extraction into L1Topo (pre-phase1)

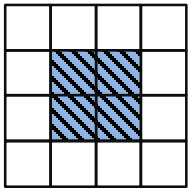
Phase-1: jet feature extractor jFEX

- Improve on jet finding (and MET measurement)
- Finer granularity
- LAr signals optically from digital processor system
- TileCal options

jFEX input data

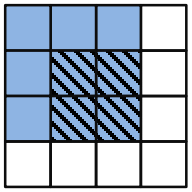
- Fibre optical inputs only
- Fibre bundles via patch panel / fibre re-bundling stage
- Granularity .1×.1 (η×φ)
- One electromagnetic, one hadronic tower per η×φ bin
- Unlike eFEX, no "BCMUX" scheme possible due to consecutive non-zero data
- Baseline 6.4 Gb/s line rate, 8b/10b encoding,
  → 128 bit per BC
- 16bit energy per tower, 8 towers per fibre
- LAr data from DPS
- Tile … see later presentations

Algorithms, now…

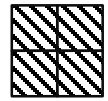


Sliding window algorithm (sliding in φ, η)

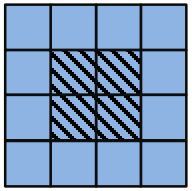
Operate on jet elements (towers) 0.2 x 0.2



Find and disambiguate ROIs sized 0.4 x 0.4



Calculate jet energy in three differently sized windows (programmable), up to 0.8 x 0.8

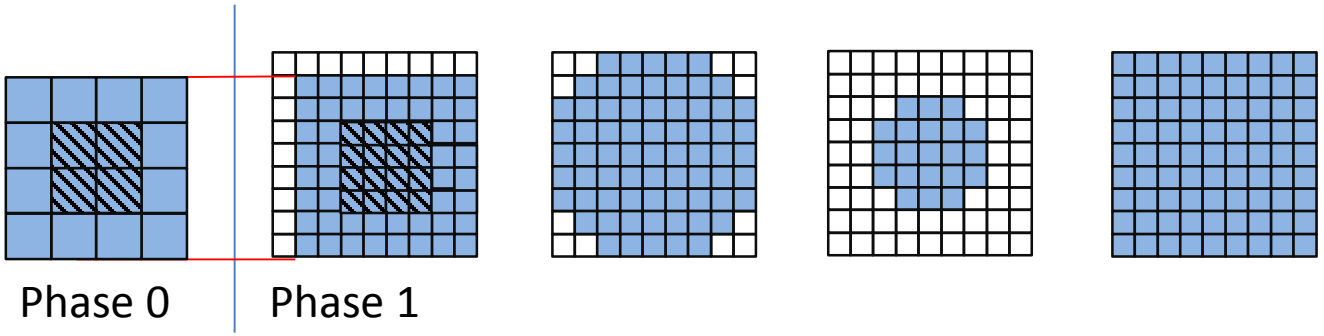


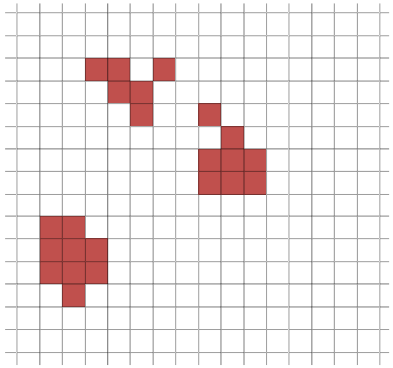
Jet size (window size) limited by environment (data duplication)

Granularity defined by arithmetic on Pre-Processor ASIC (pre-sum)

… and then

- Increase dynamic range
- Improve granularity by factor of four, to 0.1×0.1 (η×φ)
- Slightly increase environment (0.9 × 0.9 baseline)
- Allow for flexibility in jet definition (non-square jet shape, Gaussian filter, …)
- Fat jets to be calculated from high granularity small jets
- Optionally increase jet environment

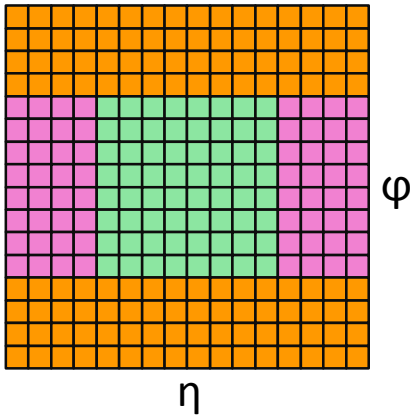




Data replication

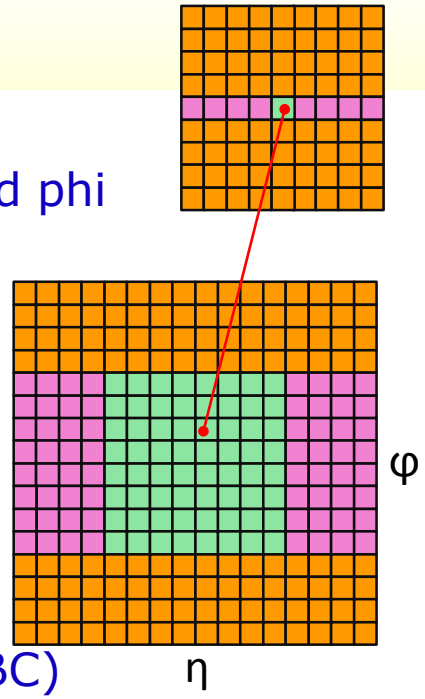
Sliding window algorithm requiring large scale replication of data

- Forward duplication only (fan-out), no re-transmission
- Baseline: no replication of any source into more than two sinks
- **Fan-out in eta** handled at source only (DPS)
  - Transmit **"core"** and **"environment"** data
  - Duplication at the parallel end (on-FPGA), using additional Multi-Gigabit Transceivers
  - Allowing for differently composed streams
  - Minimizing latency
- **Fan-out in phi** handled at destination only
  - Baseline "far end PMA loopback"
  - Looking into details and alternatives
- N.B. phi strip vs. eta strip organisation tbd.



jFEX partitioning

Algorithm requiring environment of 0.9×0.9 around each tower to be processed → +/- 4 neighbours in eta and phi

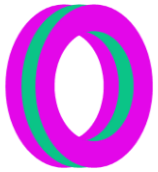


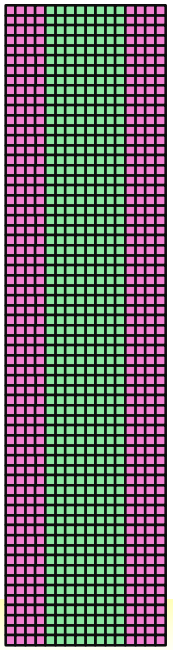
Processor FPGAs

- **core of 0.8×0.8**
- Fully duplicated data in both eta and phi
- Total of 1.6×1.6 worth of data required
- 256 bins @ 0.1×0.1 granularity
- separate e/m + had channels → 512 numbers (16-bit energies)
- That equals 64 on-chip receivers @6.4Gb/s (128 bit/lane/BC)
- Due to 100% on-board duplication, 32 of them are driven from a fibre

Processor modules

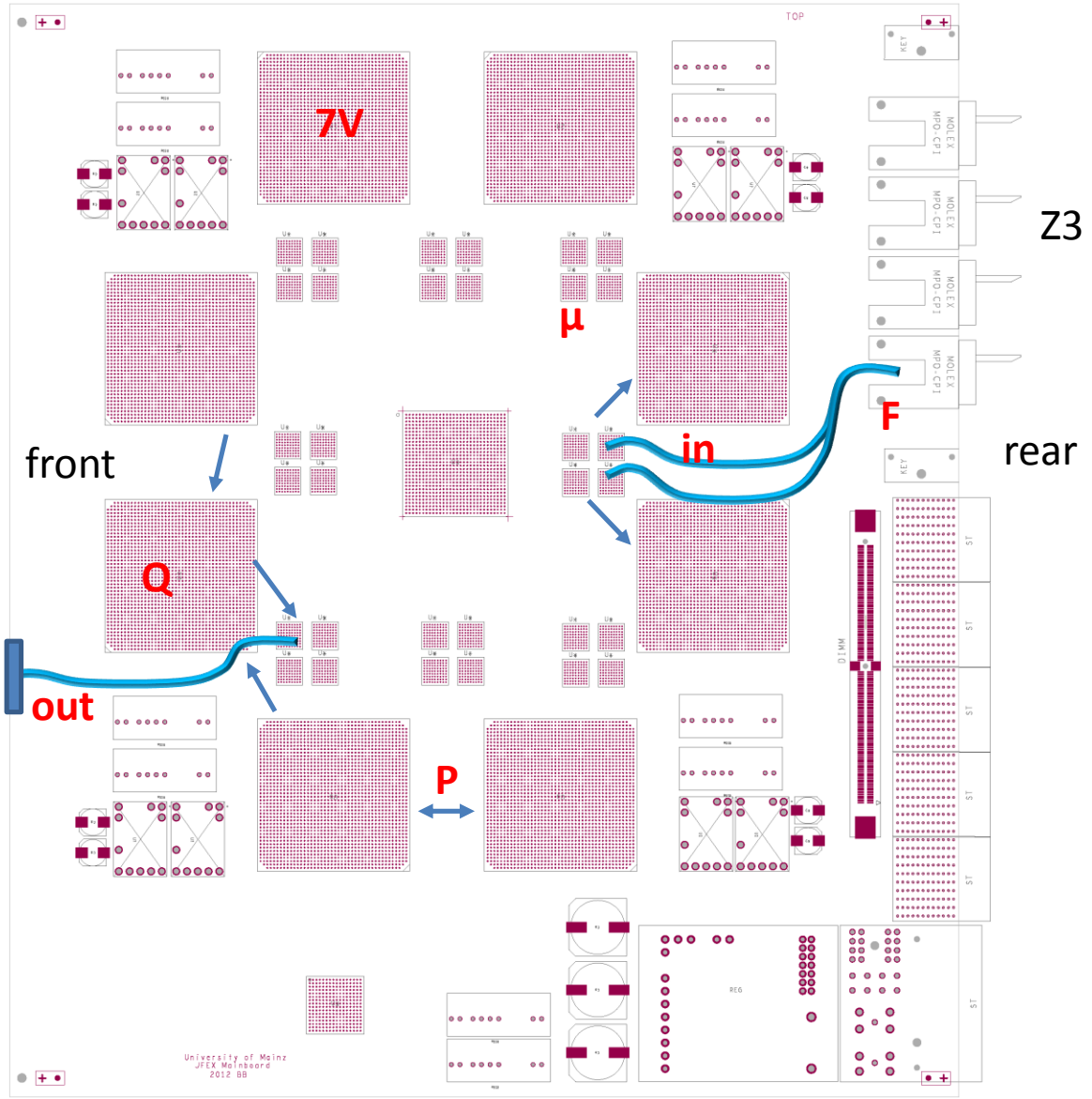
- Processing strip along phi
- Receiving fully duplicated data in eta from DPS
- Module covering full phi (8×0.8), limited eta range of .8
- Carrying 8 FPGAs
- → total of 8×32=256 fibres coming in
- 22 × 12-way opto modules **"MicroPOD"** high density receivers
- Four 72-way fibre connectors ("MPO/MTP")



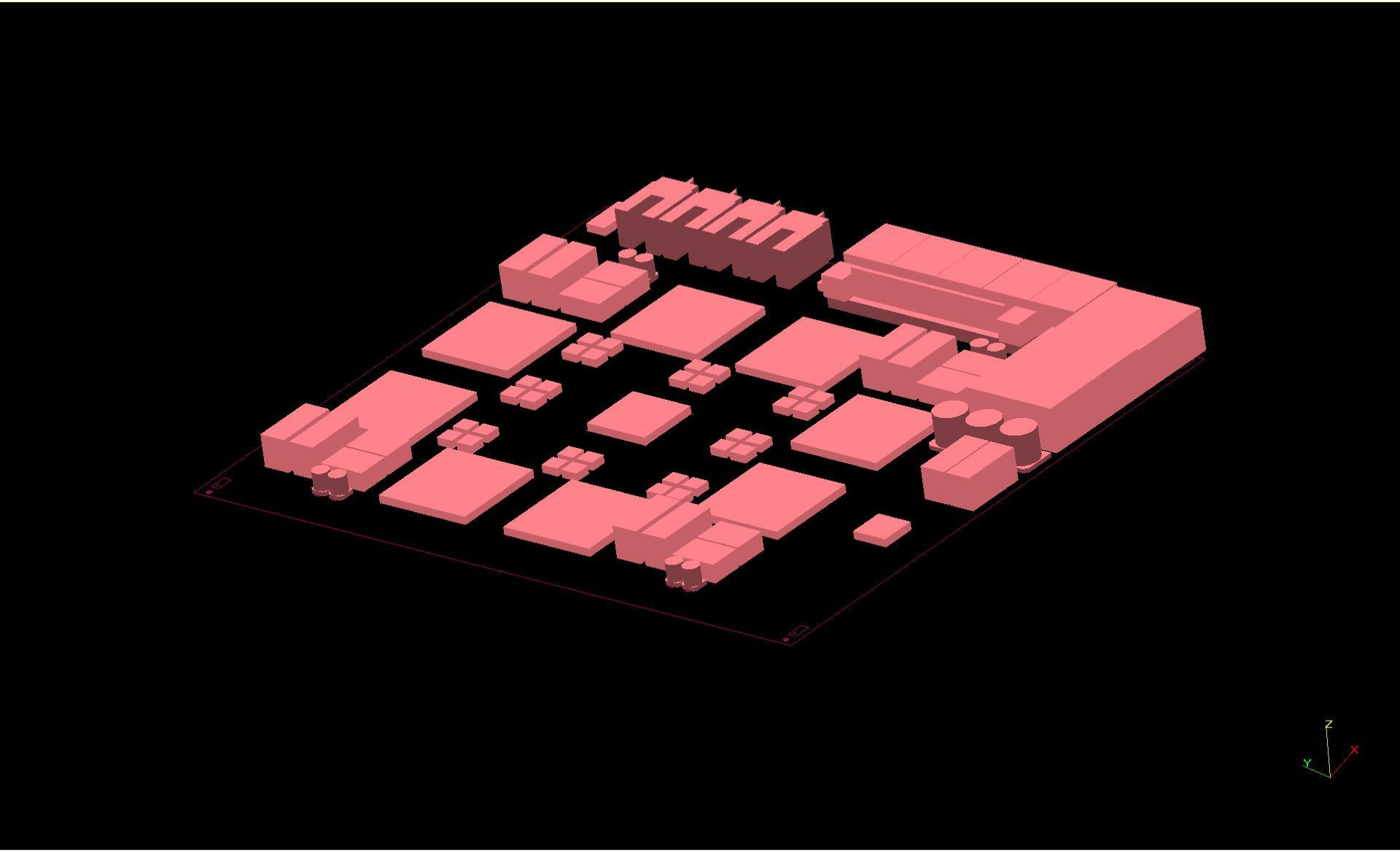


How to fit on a module ?

- AdvancedTCA format
- 8 processors (~XC**7V**X690T)
- 4 microPOD sockets each **µ**
  (including spare output)
- Opto connectors in
  Zone 3
- Fibre bundles from rear **F**
- fan-out via "far end PMA loopback" **P**
- consolidation of results on one of the processors **Q**
  (alternatively direct output)
- Output to front panel
- Small amount of module control logic / non-realtime (ROD)
- Maximise module payload with help of small-footprint ATCA power brick and tiny IPMC mini-DIMM



…and 3-d



Some considerations…

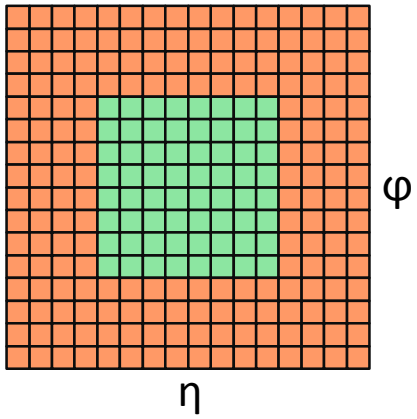
- jFEX relies on "MicroPOD" high-density optical devices
  - Electro-optical engine identical to popular "MiniPOD"s
  - Currently looking into mechanical and thermal issues
  - In contact to manufacturer to benefit from recent developments there
  - MicroPODs small enough to provide additional direct output from each processor FPGA if required (for fat jet determination on L1Topo module)

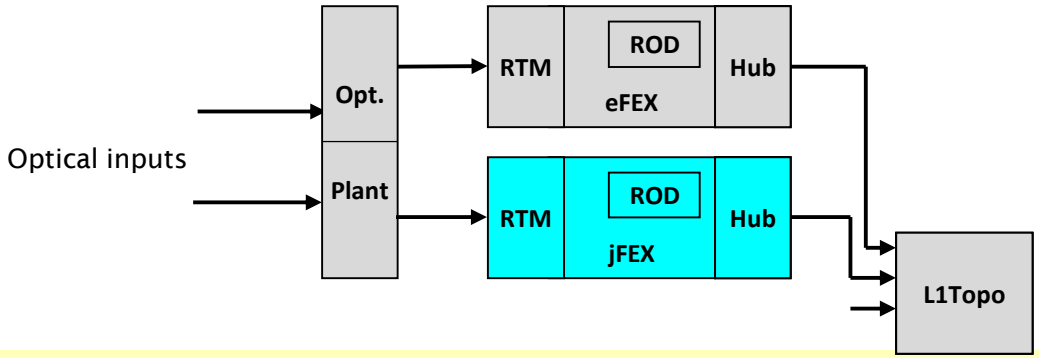
- 6.4 Gb/s baseline seems rock solid
- Fibre and module density are high but feasible
- Aim at higher line rates (currently FPGAs support 13 Gb/s, MicroPOD 10 Gb/s)
  - Allow for even finer granularity / larger jets / smaller FPGA devices :
  - If digital processor baseline allows for full duplication of 6.4Gb/s signals, the spare capacity, when run at higher rate, can be used to achieve a replication of more than 2-fold, so as to support a larger jet environment.

- The jFEX shall be compatible to phase 2
  - might affect organisation of input links (eta strips vs. phi strips)
  - Organisation of input links to be sorted out anyway

jFEX system

- Need to handle both fine granularity and large jet environment (minimum 0.9×0.9)
- Require high density / high bandwidth to keep input replication factor at acceptable level (3/4 of all FPGA inputs are duplicates)
- Fit in 8 modules / 12 modules
- Single ATCA shelf
- Sharing infrastructure with eFEX
  - Handling / splitting of fibre bundles
  - ROD design
  - Hub design
  - RTM





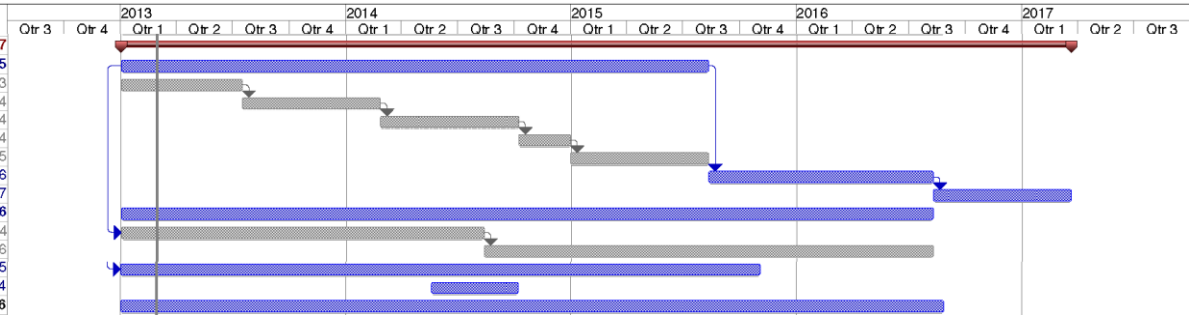
Firmware and (control / test) software

- high speed infrastructure (MGT)
- data conditioning (alignment/40Mbps/masks/pre-sums)
- thresholding scheme
- default jet algorithm (sliding window)
- advanced algorithms: jets, fat taus, ...
- energy sums
- board level merger / topology object formation and selection
- DAQ/ROI interface / embedded ROD (f/w, s/w)
- low level control (ATCA / IPMC to FPGA paths) f/w, s/w
- module (high level) control: register maps / IPBus and interfaces (f/w, s/w)
- Alignment control / monitoring / diagnostics / playback / spy incl. s/w
- TTC interface / embedded TTC
- in situ configuration update scheme (f/w, s/w)

*Firmware requiring large amount of corresponding software, PC based / embedded processor. Partitioning in firmware vs. software not currently defined. Significant effort required on module and system tests at CERN.

Schedule / Effort

ID	Task Name	Duration	Start	Finish
1	jFEX	1100 days	Tue 01/01/13	Mon 20/03/17
2	Prototype	680 days	Tue 01/01/13	Mon 10/08/15
3	Engineering specification	7 mons	Tue 01/01/13	Mon 15/07/13
4	Schematic entry	8 mons	Tue 16/07/13	Mon 24/02/14
5	Layout + PCB Simulation	8 mons	Tue 25/02/14	Mon 06/10/14
6	Manufacture	3 mons	Tue 07/10/14	Mon 29/12/14
7	Commissioning	8 mons	Tue 30/12/14	Mon 10/08/15
8	Pre-Production	13 mons	Tue 11/08/15	Mon 08/08/16
9	Production	8 mons	Tue 09/08/16	Mon 20/03/17
10	Firmware	940 days	Tue 01/01/13	Mon 08/08/16
11	Interface and Control	21 mons	Tue 01/01/13	Mon 11/08/14
12	Algorithmic	26 mons	Tue 12/08/14	Mon 08/08/16
13	ATCA (+TTC) module control	37 mons	Tue 01/01/13	Mon 02/11/15
14	RTM: design -> commissing	5 mons	Tue 20/05/14	Mon 06/10/14
15	Firmware	954 days	Tue 01/01/13	Fri 26/08/16



Plus installation/commissioning/system tests thereafter.

Milestones PDR Q3/2013
FDR Q3/2015
PRR Q3/2016

Requirements

- jFEX hardware, firmware: total of 17 FTE over 6 years, rather evenly spread until production…
- JMM mezzanine renewal (h/w+f/w) including TileCal fibre interface: total of 5 FTE over 6 years
- Integration, installation, commissioning (jFEX share): 6 FTE / 6 years

Known available effort:

Mainz is able to cover all required work on hardware, firmware and installation/commissioning

Total effort available: Physicist 5FTE, Engineer 1FTE per year

Conclusion

- The 8-module, single crate jFEX seems possible with today's technology
- Use of MicroPODs challenging (thermal and mechanical)
  - o/e engine is the same as in popular MiniPODs
- Phi ring scheme (→IDR) allows for fine granularity and large environment @ 6.4Gb/s and 100% duplication of input data
- Larger environment achieved at baseline data rate by eta strip partitioning (2*6 modules, 1 crate)
- Which scheme is more suitable for phase-2 ?
- Even finer granularity and / or larger jets possible at higher transmission rates
- DPS needs to handle the required duplication
  - in eta (phi ring scheme)
  - in phi (eta strip scheme)

Details of fibre organization and content to be defined.

Started work on detailed specifications, in parallel exploring higher data rates…