jFEX baseline

Uli

PRISMA

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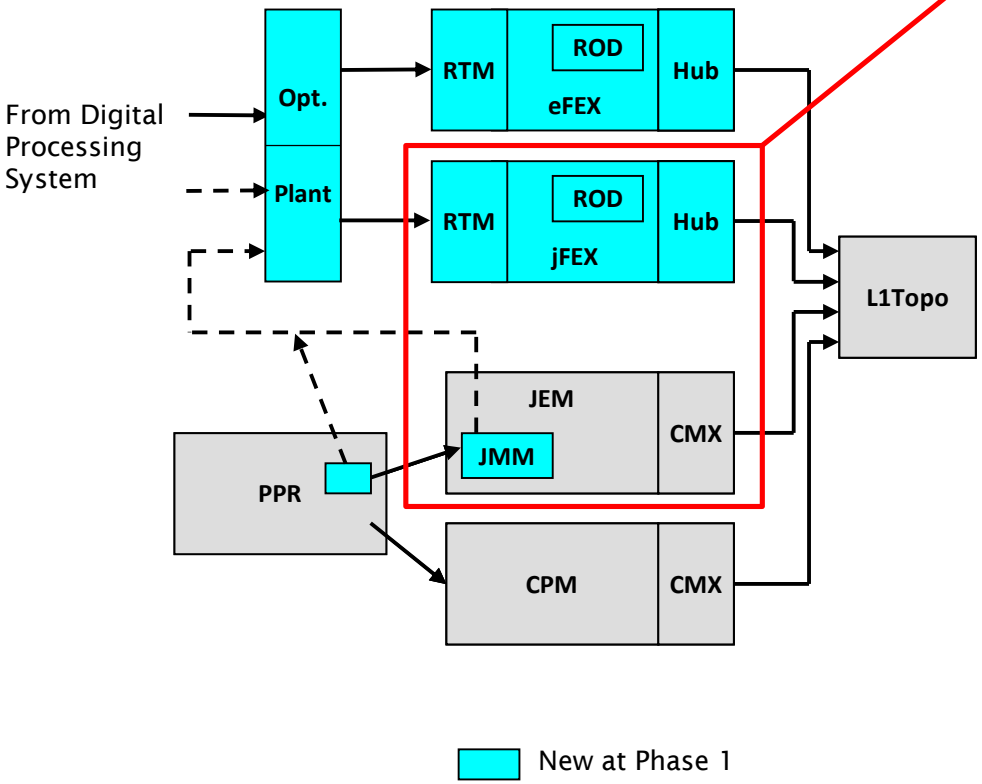
Intro: L1Calo Phase-1 System / Jets



Jets

Phase-0

- Jet elements 0.2 x 0.2 (η×φ) (pre-processor)
- Sliding window processor for jet finding JEP / JEM
- Jet multiplicity determination
- Jet feature extraction into L1Topo (pre-phase1)

Phase-1: jet feature extractor jFEX

- Improve on jet finding (and MET measurement)
- Finer granularity

jFEX input data

- Fibre optical inputs only
- Fibre bundles via patch panel / fibre re-bundling stage
- Granularity .1×.1 (η×φ)
- One electromagnetic, one hadronic tower per η×φ bin
- Baseline 6.4 Gb/s line rate, 8b/10b encoding,
  → 128 bit per BC
- 16bit energy per tower, 8 towers per fibre

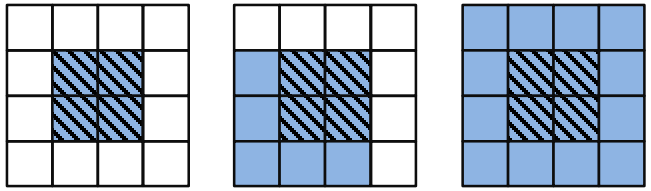
- LAr data from DPS
- Tile … options…

Sliding Window Algorithms

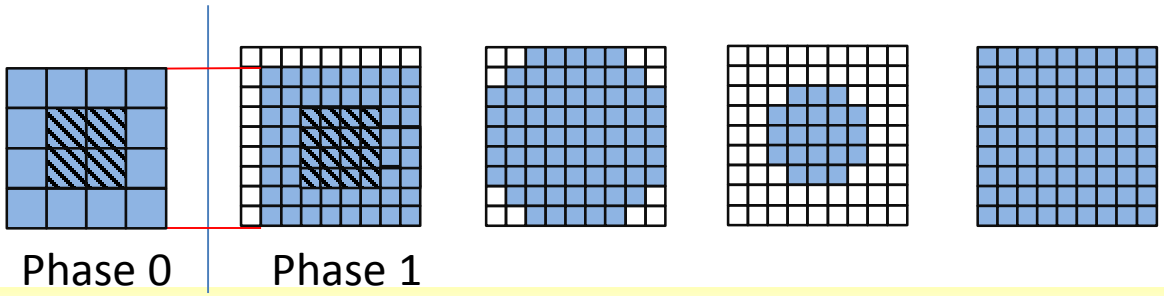
Jet elements (towers)

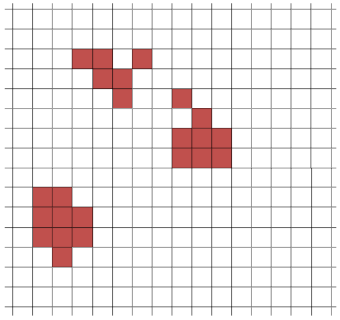
ROIs

environment



- Increase dynamic range
- Improve granularity by factor of four, to 0.1×0.1 (η×φ)
- Slightly increase environment (0.9 × 0.9 baseline)
- Allow for flexibility in jet definition (non-square jet shape, Gaussian filter, …)
- Fat jets to be calculated from high granularity small jets
- Optionally increase jet environment

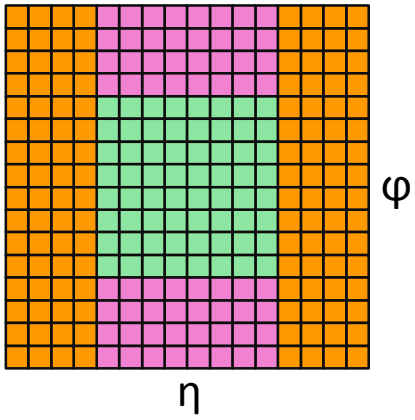




Data replication

Sliding window algorithm requiring large scale replication of data

- Forward duplication only (fan-out), no re-transmission
- Baseline: no replication of any source into more than two sinks
- Eta-strip organisation
- **Fan-out in phi** handled at source only (DPS)
  - Transmit **"core"** and **"environment"** data
  - Duplication at the parallel end (on-FPGA), using additional Multi-Gigabit Transceivers
  - Allowing for differently composed streams
  - Minimizing latency
- **Fan-out in eta** handled at destination only
  - Baseline "far end PMA loopback"
  - Looking into details and alternatives
- N.B. module orientation in phi vs. eta strip tbd. Above scheme is baseline !



Module partitioning

Give up on phi ring scheme

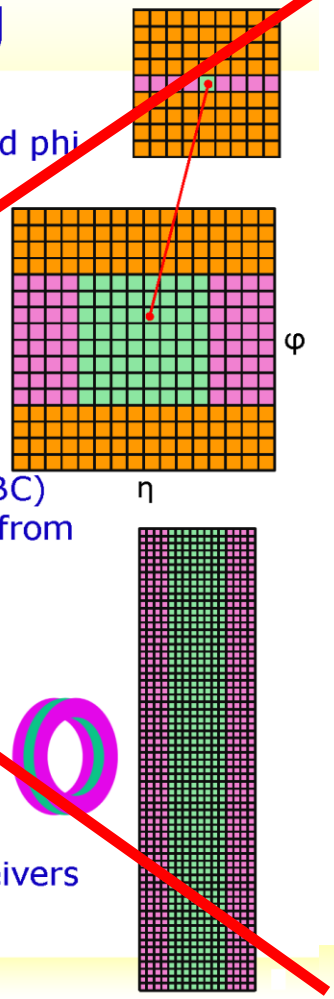
Baseline : Go for strips along eta !

jFEX module partitioning

Algorithm requiring environment of 0.9×0.9 around each tower to be processed → +/- 4 neighbours in eta and phi

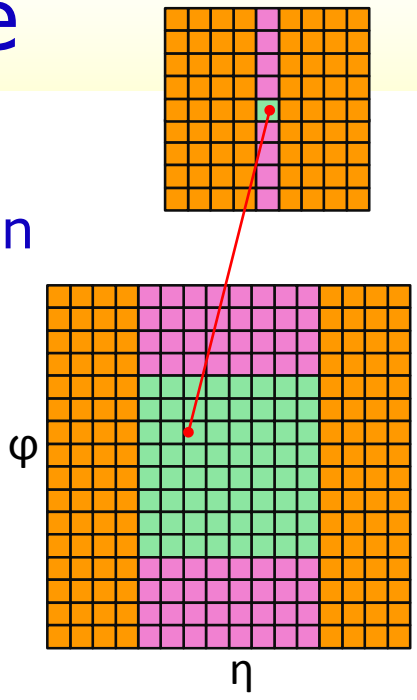
Processor FPGAs
- **core of 0.8×0.8**
- Fully duplicated data in both eta and phi
- Total of 1.6×1.6 worth of data required
- 256 bins @ 0.1×0.1 granularity
- separate e/m + had channels → 512 numbers (16-bit energies)
- That equals 64 on-chip receivers @6.4Gb/s (128 bit/lane/BC)
- Due to 100% on-board duplication, 32 of them are driven from a fibre

Processor modules
- Processing **phi ring**
- Receiving fully duplicated data in eta from DPS
- Module covering full phi (8×0.8), limited eta range of .8
- Carrying 8 FPGAs
- → total of 8×32=256 fibres coming in
- 22 × 12-way opto modules **"MicroPOD"** high density receivers
- Four 72-way fibre connectors ("MPO/MTP")



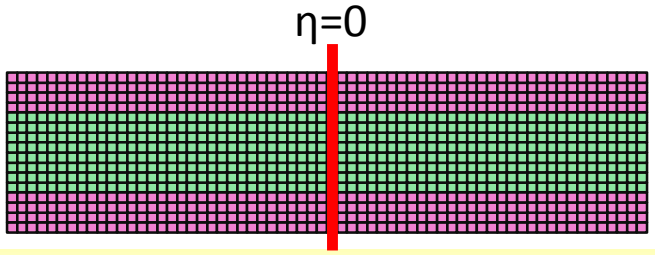
jFEX module partitioning baseline

Algorithm requiring environment of 0.9×0.9 around each tower to be processed → +/- 4 neighbours in eta and phi



Processor modules

- Process strips along eta
- Receive fully duplicated data in phi from DPS
- 8 modules covering half of eta, phi quadrant each
- Most cells duplicated in a regular way at both source and sink
- "Irregular" duplication at **η=0**
- (Current) detector cabling has lower latency around η=0 due to cable **path**
- Benefit from this latency reserve and use for additional optical fan-out (re-transmission)



jFEX baseline partitioning

Processor modules

- Half eta × phi quadrant per module
- Total of ~32 × 16 bins × 2 × 2 (upstream duplication, e/h)
- ~256 incoming fibres @ 6.4Gb/s baseline
- 22 × 12-way opto modules "MicroPOD" high density receivers
- Four 72-way fibre connectors ("MPO/MTP")
- Note: further connectivity required for duplication at η=0: either front (re-transmission) or back (separate active optical fanout station)

Processor FPGAs

- Core of up to 1.2×0.8 (η×φ), plus environment 0.8×0.8
- 20 × 16 bins → 80 high speed links
- 6 large FPGAs per module

Baseline and options

Phi quadrant baseline driven by need for a rock solid design:

- Line rate limited to 6.4 Gb/s only
- Avoid extremely dense module
- Sufficient $\eta \times \varphi$ coverage at module level to allow for increase of environment » baseline of 0.9×0.9
- Orientation along eta might better match Tilecal in phase 2

Backup

- In case of problems with $\eta=0$ - duplication go for full eta, phi octant scheme

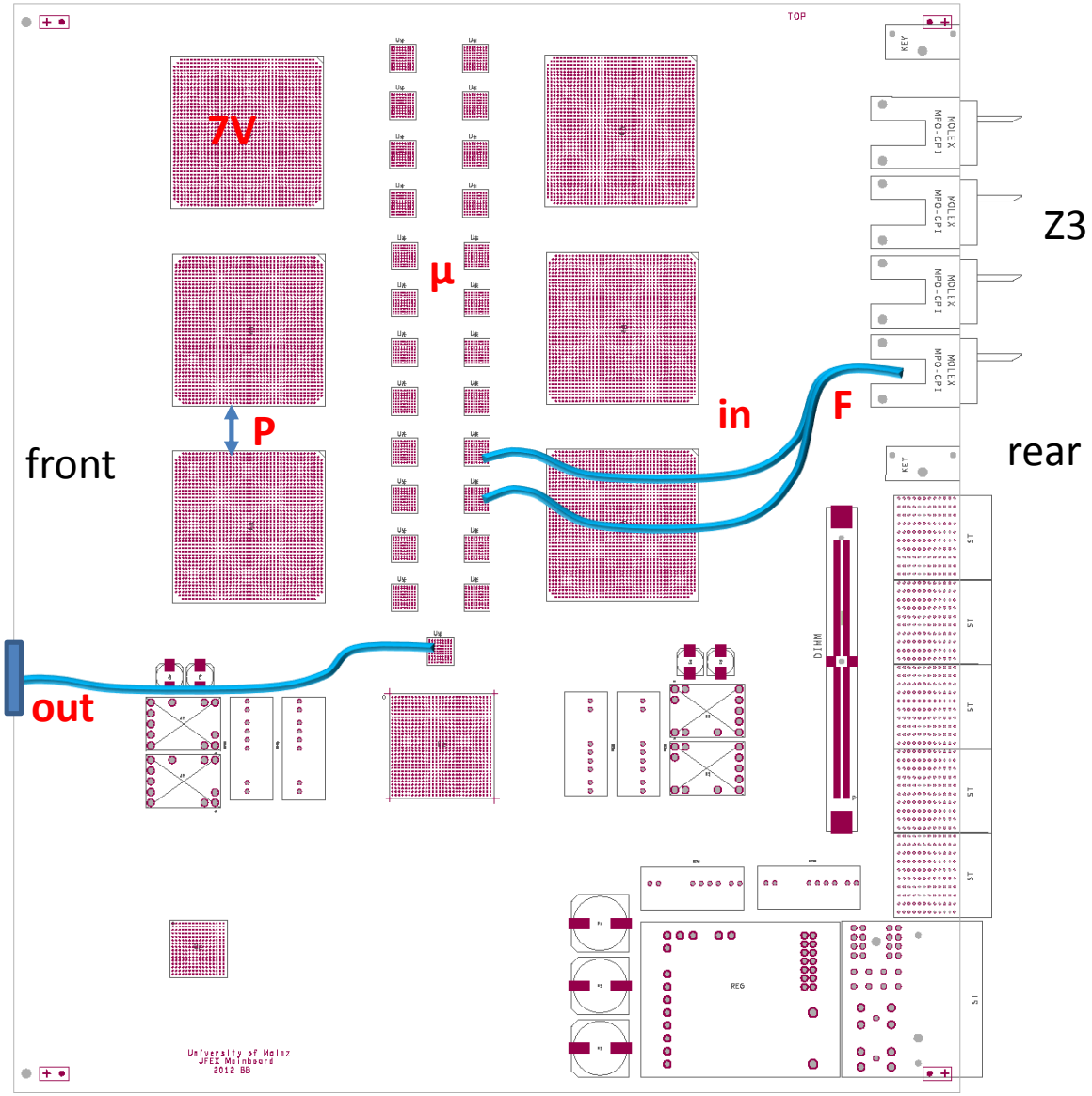
Options

- Continue work on higher link speed
- Continue work on duplication schemes
- Consider slightly larger/more FPGAs

→ Increase environment beyond 0.9×0.9

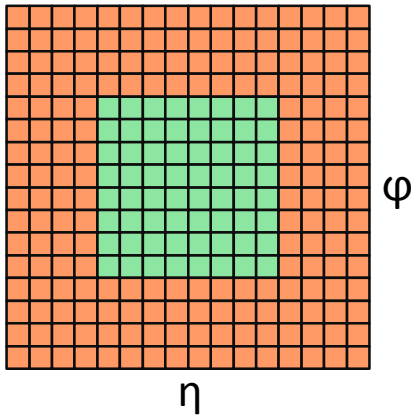
How to fit on a module ?

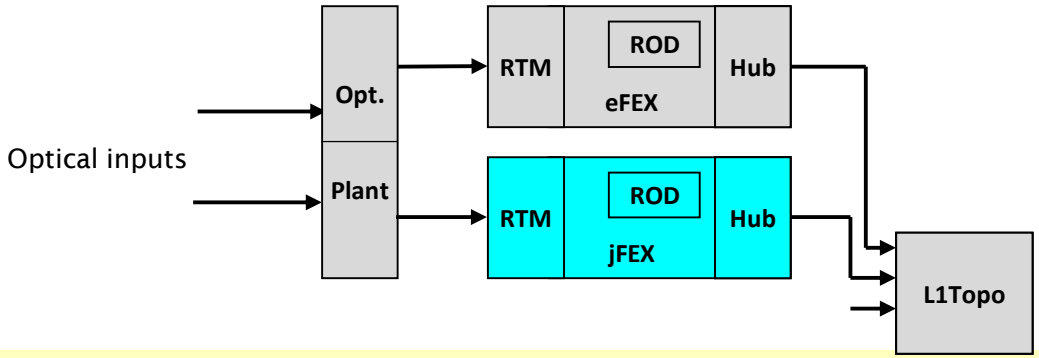
- AdvancedTC A format
- 6 processors XC**7V**X690T
- 4 microPOD sockets each **µ**
- Opto connectors in Zone 3
- Fibre bundles from rear **F**
- fan-out via "far end PMA loopback" **P**
- Output to front panel
- Small amount of module control logic / non-realtime
- Maximise module payload: small-footprint ATCA power brick, tiny IPMC mini-DIMM



jFEX system (baseline)

- Need to handle both fine granularity and large jet environment (minimum 0.9×0.9)
- Require high density / high bandwidth to keep input replication factor at acceptable level (~3/4 of all FPGA inputs are duplicates)
- Fit in 8 modules
- Single ATCA shelf
- Sharing infrastructure with eFEX
  - Handling / splitting of fibre bundles
  - Some communalities in ROD design
  - Hub design
  - RTM





Some remarks on baseline

- FPGA density reduced wrt previously presented phi ring scheme
- Still very dense design
- FPGA count might grow again for larger jet option
- Real-time circuitry has absolute precedence over non-real-time components
  - RODs tiny mezzanines or even external modules
  - Any TTC solution must be minimum footprint
  - Power and ATCA control minimized in floor-plan shown
- Baseline design would probably allow for low-latency direct output into L1Topo (48 fibres total)
- Output consolidation possible at some latency penalty

Conclusion

- 8-module, single crate jFEX possible with today's technology
- Use of MicroPODs challenging (thermal and mechanical)
  - o/e engine is the same as in popular MiniPODs
- Eta strip (phi quad) scheme allows for fine granularity and large environment 0.9×0.9 @ 6.4Gb/s
- Relies on lower latency of incoming data near η=0
- With 100% duplication of input data at source there is enough environment data available on-module for larger environment
- Higher transmission rates
- DPS needs to handle the required 100% duplication in phi

Details of fibre organization and content to be defined.

Started work on detailed specifications, in parallel exploring higher data rates…