jFEX ROD bandwidth

- Baseline jFEX - phi quadrant/eta strip:
- 6 FPGAs × 80 input links @ 6.4Gb/s → 480 links
- DAQ data volume probably dominated by inputs
- 40MHz → 100kHz : require 480/400 ROD links **per time slice** sent.
- Scaling up accordingly for phase 2
- Assume inputs and DAQ outputs same link type and speed
- → 1.2-6 MGT links into ROD at phase 1
- Allow for some headroom to avoid need for excessively large local buffer
- Local buffer **needs** to be implemented on processor FPGAs !

- For the time being assume this input into some external ROD modules