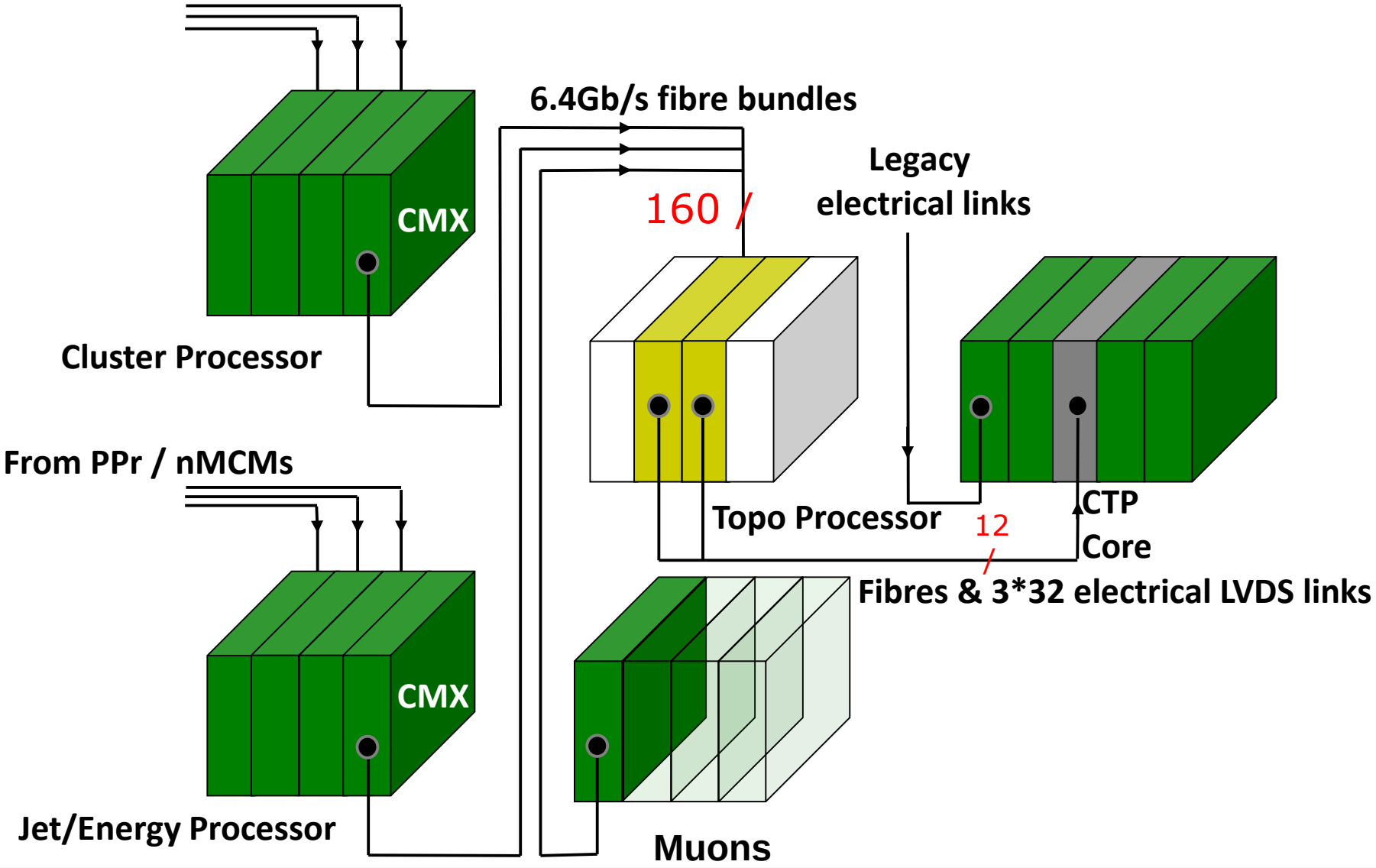
L1Topo Hardware Status & Plans

B.Bauß, V.Büscher, U.Schäfer, E.Simioni,
S.Tapprogge, A. Vogel

Topology 2013/14 (RTDP)



Topology Processor – Pre-phase1

- Correlating trigger objects (TOBs: jets, clusters, muons)
- Single AdvancedTCA crate
- Up to three modules running separate algorithms concurrently
  - Fibre-optical input via Rear Transition Module on 48-way connectors
  - MiniPOD optical receivers
  - Input bandwidth 820 Gb/s @ 6.4Gb/s (2014 baseline rate)
  - Two high-end FPGA processors (7-series) working concurrently on separate copies of the TOBs
  - Additional parallel inter-FPGA real-time links (> 200Gb/s)
- Both fibre bundle and low latency LVDS into CTPcore
- Some critical circuitry on mezzanine, to allow for later mods

- Well prepared for phase 1 / 2:
  - Module control and readout compatible to L1Calo/FEX scheme
  - Accept line rates above 6.4Gb/s from future processors (FEXes, muons)

Topo Processor – Prototype

- Fully **ATCA** compliant
  - Form factor, power scheme, IPMC, base interface (Ethernet)
- Real-time input path capable of multiple data rates
  - One LHC bunch clock derived reference clock for receivers and transmitters
  - Segmented clock trees with multiple crystal-based frequencies (receiver references only)
- Total of 18 MiniPOD sockets (real-time input and output, readout)
- Via four 48-way backplane connectors (realtime inputs) and front panel
- XC7V690T FPGAs (first prototype: XC7V485T)
- Interlinked by 238-way LVDS path
- 12-way optical output to CTP
- 32-way electrical (LVDS) output to CTP via mezzanine
- Module control via “Kintex” control FPGA
- Embedded ROD on control FPGA
- Low-level control via IPMC dimm
- Spare socket for “MARS” module

L1Topo

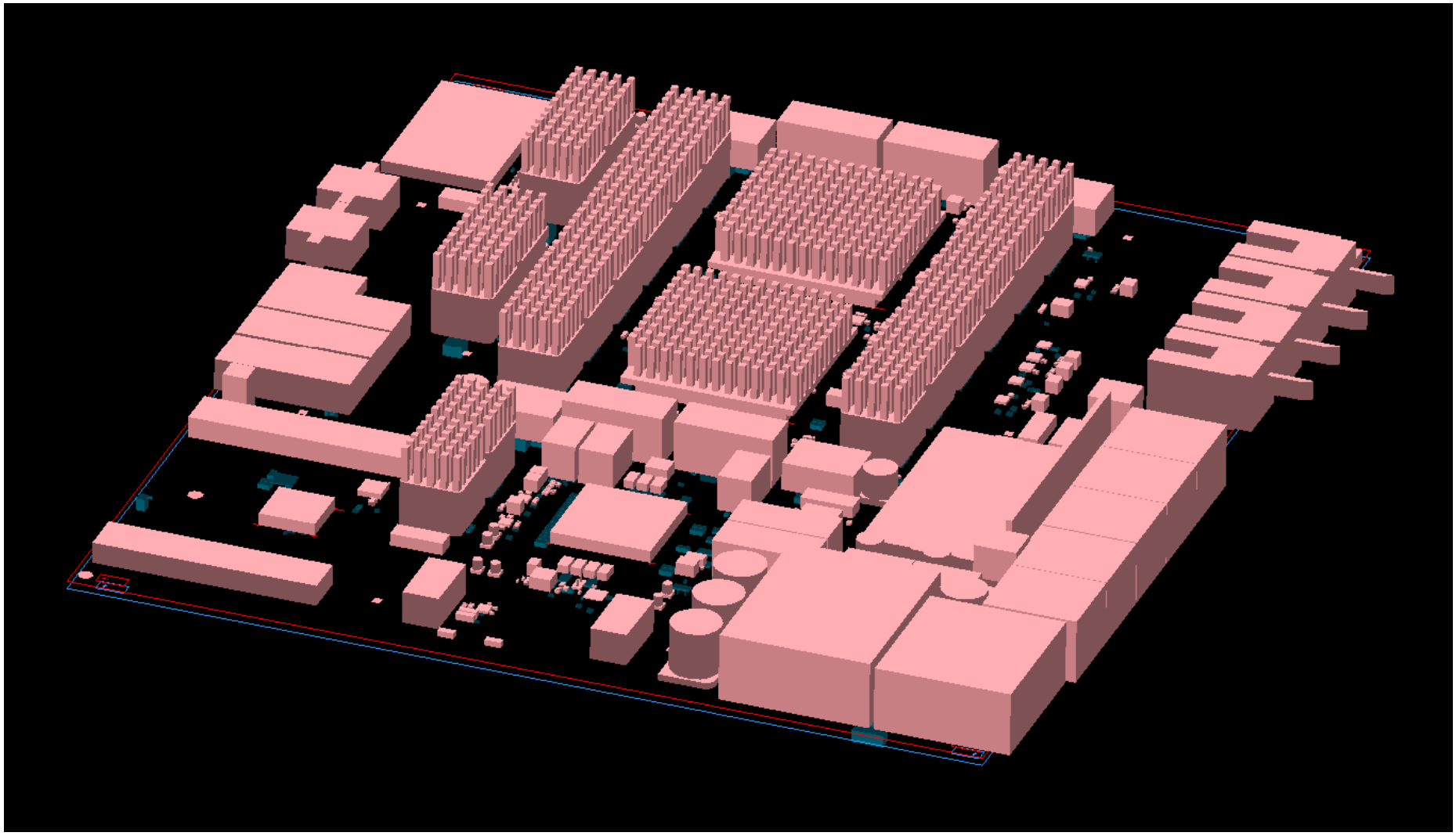
- FPGA configuration via SystemACE or SD card
- Optional use of SFP links into L1Calo RODs for initial debug (ROD neutral firmware)

Minor modifications expected for production modules

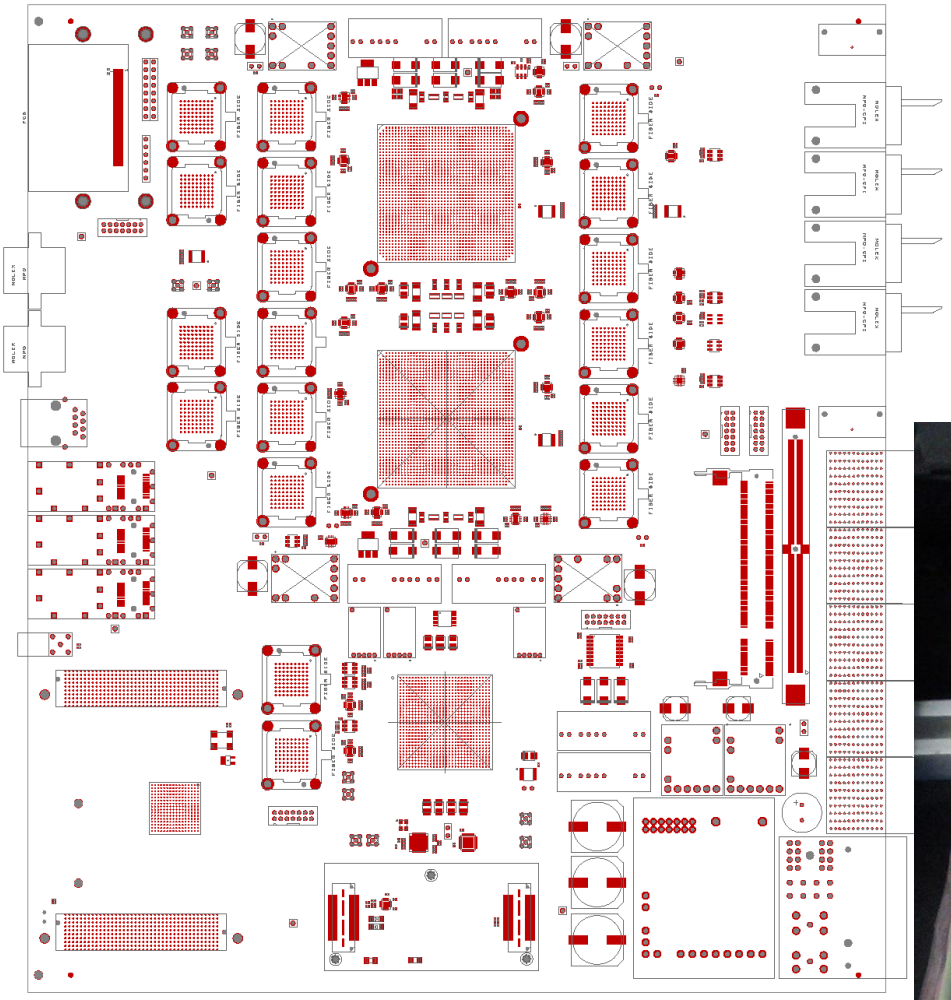
- Remove “MARS” module option
- Possibly remove SFP link option
- Possibly increase bandwidth to allow for AXI4-stream interconnect to processor FPGAs (see presentation later today)
- Simplify extension module scheme
- Add optional readout and TTC connectivity for compatibility with L1Calo Phase-1 scheme (FEXes)

Final modifications will be discussed with reviewers at PRR

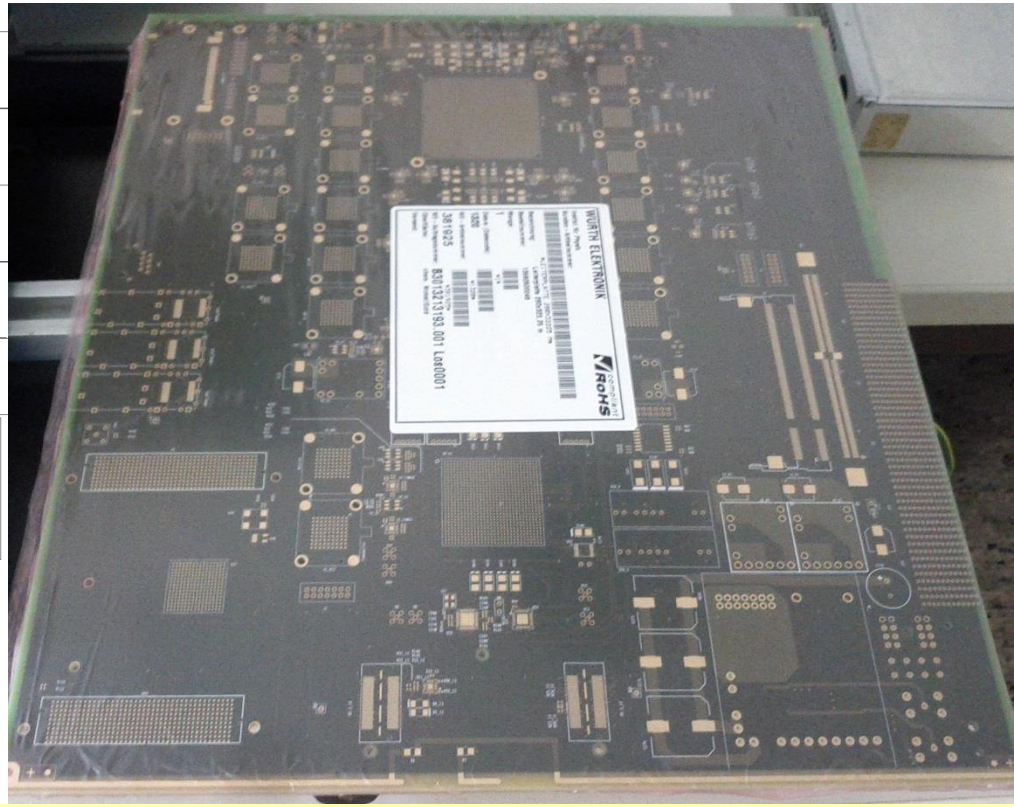
3–d



L1Topo Prototype

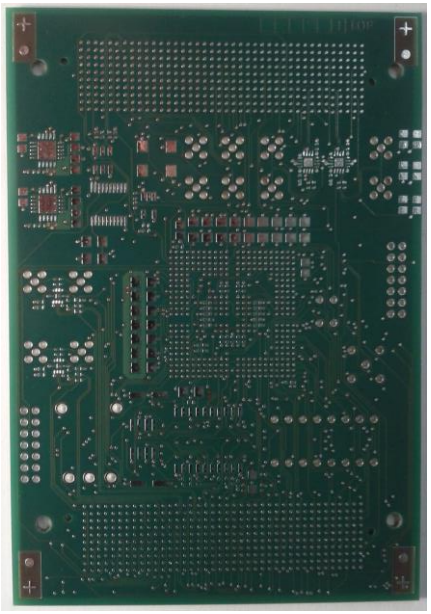


Floorplan and PCB



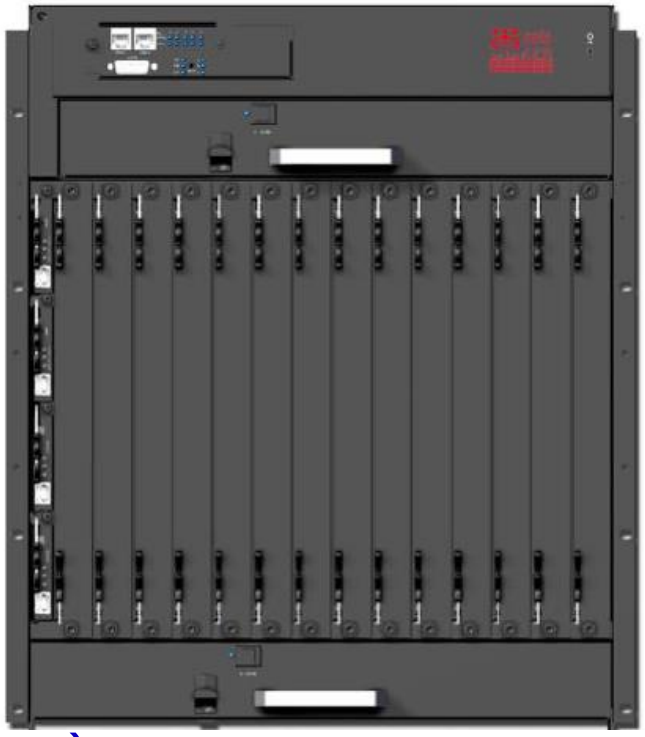
Hardware status

- April 10 L1Topo PCB submission (3 weeks)
- Production issues
- Eventually three prototype PCBs received from manufacturer
- One PCB out for assembly (4 weeks) since end of May
- Delayed to probably mid July
- Bruno will start initial tests (smoke test, boundary/scan) after vacation early August
- Initial version of extension mezzanine:
  - Bridging b/scan and control paths
  - Connecting TTC/clocks and I2C buses
  - PCB available
  - Assembly in-house early August
- No IPMC dimm available yet. Bring up L1Topo on the bench initially



Hardware status

- Eduard trying to find suitable ATCA crate (vertical air flow) for operation in USA15
- 14 slots
- 14U(Height) × 10U (Width) × 9-10U (Depth)
- Base interface: Dual Star supporting 10/100/1000 Base-T Ethernet
- Fabric interface: Full mesh available, 40 Gbps/chan
- Shelf manager included
- Dual redundant IPMC support
- -48 VDC, five feeds per PEM (up to 250 Amp)
- ~ 14K€ euro including NRE cost
- Up to 10 self cooled, AC hot swappable PSU (not included)



Shelf can be purchased once funds released

L1Topo – some Milestones

- Jun 2012 PDR
- Jan 2013 Internal review
- May 2013 FDR
- Oct 2013 start prototype tests @ CERN
- Oct 2013 PRR
- Jan 2014 assembly of production module finished
- Apr 2014 start production module tests @ CERN
- End 2014 commissioning done

Further news

- Firmware and online S/W status will be discussed separately
- While waiting for L1Topo prototype . . .

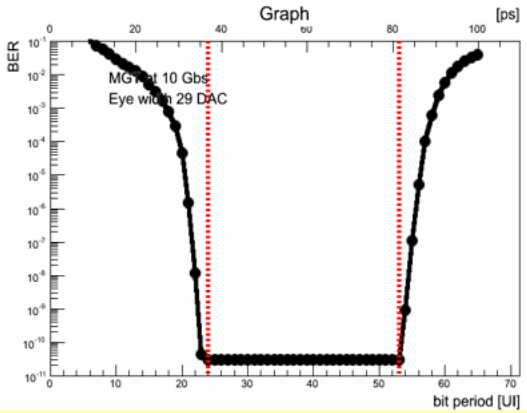
→ Work on I2C based component control (Eduard)

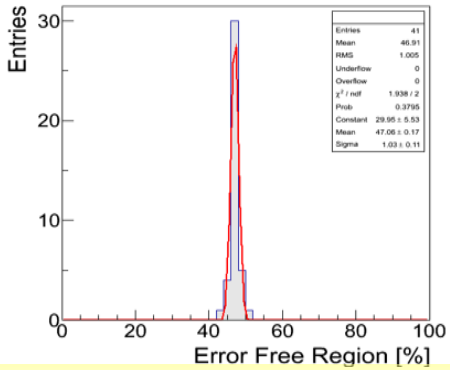
→ Systematic link BER tests @ 10Gbps / 7-bit PRBS pattern on MiniPOD / KC705 (Alex)

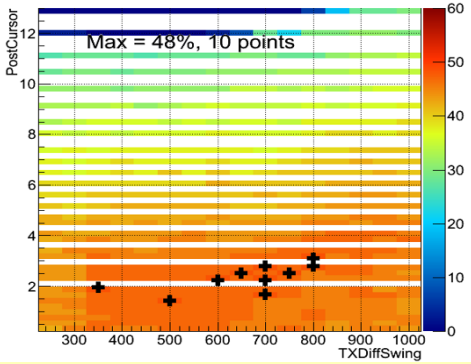
→ Repeated measurements of bath tub

→ Trying to understand pre-compensation parameters

→ Long-term tests to follow…







Summary

L1Topo Prototype

- PCBs successfully done
- Assembly under way
- Tests starting in August
- At CERN in October

L1Topo Production modules

- minor modifications wrt prototype
- FDR done
- Commissioning at CERN from spring 2014

On schedule for installation during shutdown ´13/14