jFEX / baseline

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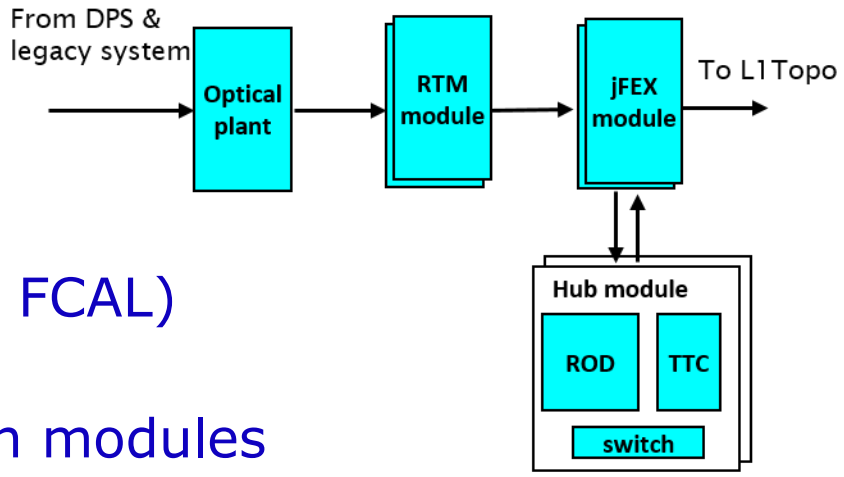
For L1Calo Mainz

jFEX system : overview

- Jet finding with sliding window algorithms
- Single AdvancedTCA shelf
- DPS feeding jFEX system via optical plant
- Readout, TTC, control via common hub modules



Eight jFEX modules

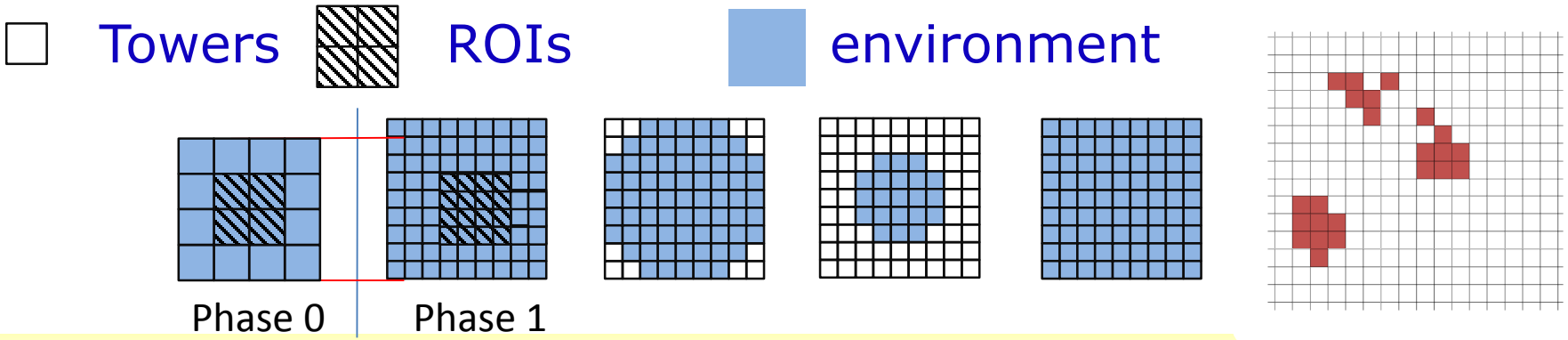
- Each covering phi octant
- 9.8 eta x 0.8 phi (Barrel, Endcap, FCAL)
- Environment in phi
- Opto fibre input via rear-transition modules
- Readout, TTC, control via backplane
- Optical output to L1Topo

Input data

- 6.4Gb/s baseline
- 8 trigger towers per fibre (4x2)

Jets: Sliding Window Algorithms

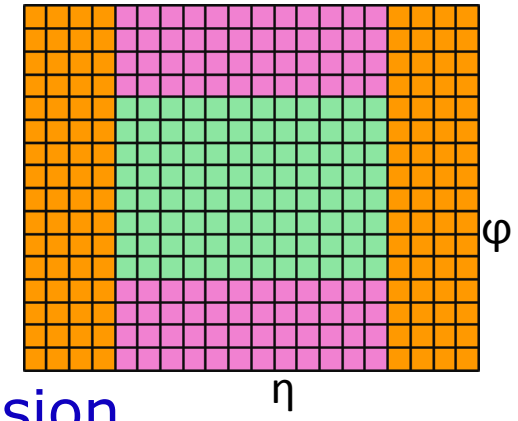
- Increase dynamic range wrt. Phase 0 scheme
- Improve granularity by factor of four, to **0.1×0.1** (η×φ)
- Slightly increase environment (**0.9 × 0.9** baseline)
- Allow for flexibility in jet definition (non-square, Gaussian filter, …
- Fat jets might be calculated from high granularity small jets at L1Topo
- Optionally increase jet environment !
- Fat tau algorithm resides in same modules



Data replication

Sliding window algorithms requiring large scale replication of data

- Forward duplication only (fan-out)
- No replication of any source into more than two sinks
- Eta-strip / phi octant organisation:
- **Fan-out in phi** handled at source only (DPS)
  - Transmit **"core"** and **"environment"** data
  - Duplicate all data using additional Multi-Gigabit Transceivers (100% duplication)
  - Maximizing signal integrity
  - Minimizing latency
- **Fan-out in eta** handled at destination only
  - Baseline "far end PMA loopback"
  - Low latency FPGA-to-FPGA re-transmission



jFEX module

Processor modules

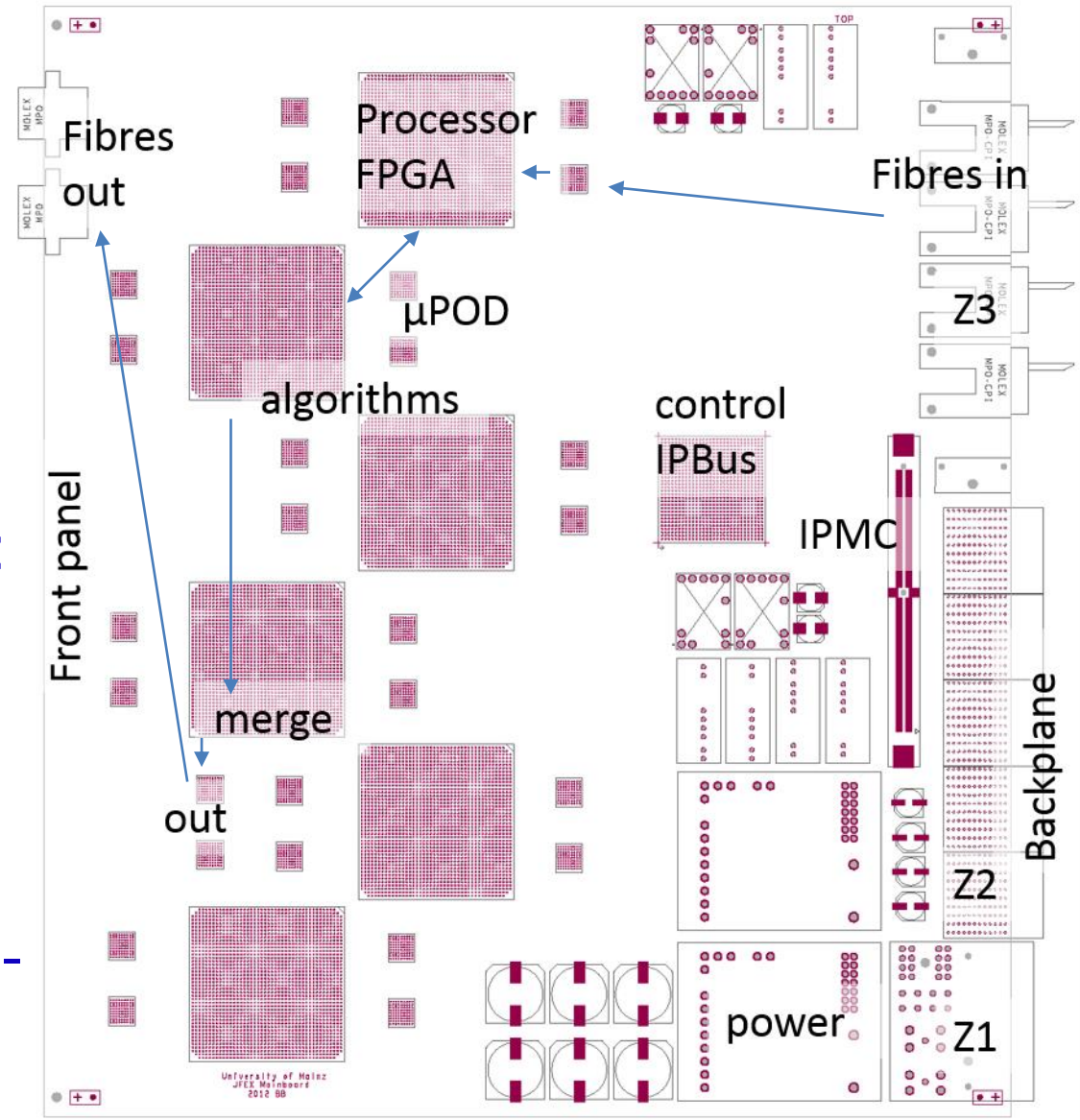
- Eta strip × phi octant : per module ~9.8 × 0.8
- Granularity 0.1 x 0.1 except FCAL
- (up to) 72 × 8 bins × 2 × 2 (upstream duplication, e/h)
- (up to) 288 incoming fibres @ 6.4Gb/s baseline
- 22(24) × 12-way "MicroPOD" high density receivers
- Four 72-way fibre connectors ("MPO/MTP")

Processor FPGAs

- Core of up to 1.2×0.8 (η×φ), plus environment 0.8×0.8
- 20 × 16 bins → 80 high speed links
- 6 large FPGAs per module
- XC7VX690T / XC7VX1140T (overlap region)

Floorplan & Details

- Input data from back
- Data duplication to neighbour FPGAs
- Feature identification
- Results to merger stage (low latency)
- Fibre output to L1Topo on front panel
- Module control via IPMC and Ethernet ("IPBus")
- Readout and timing/control via backplane
  - Hub / ROD modules
- Maximum space for real-time circuitry !



Baseline vs. options

jFEX (just like eFEX) design dominated by management of very high input data volume and duplication at system and FPGA level.

- Massive duplication affects signal integrity
- Decision in favour of a baseline data rate of 6.4 Gb/s
- However, recent link test results very promising
- Continue test programme on higher transmission rates

Higher transmission rate option strongly favoured !!!

- Build modules capable of double rate
- $4\eta \times 4\varphi$ trigger towers per fibre seems good choice
- jFEX module will be able to handle one quadrant in phi
- Full eta, 1.7 environment in phi
- Partitioning at FPGA level will require some additional work
- 1.7x1.7 jet size will be possible

Remark (triggered by yesterday's discussion)

- Pileup corrections possible with jFEX and L1Topo
- Calculate both jets and energy sums (slice along phi) on jFEX
- Perform pile-up corrections on L1Topo