JEP F/W status and plans

Uli, Pawel

JEM upgrade for run 2

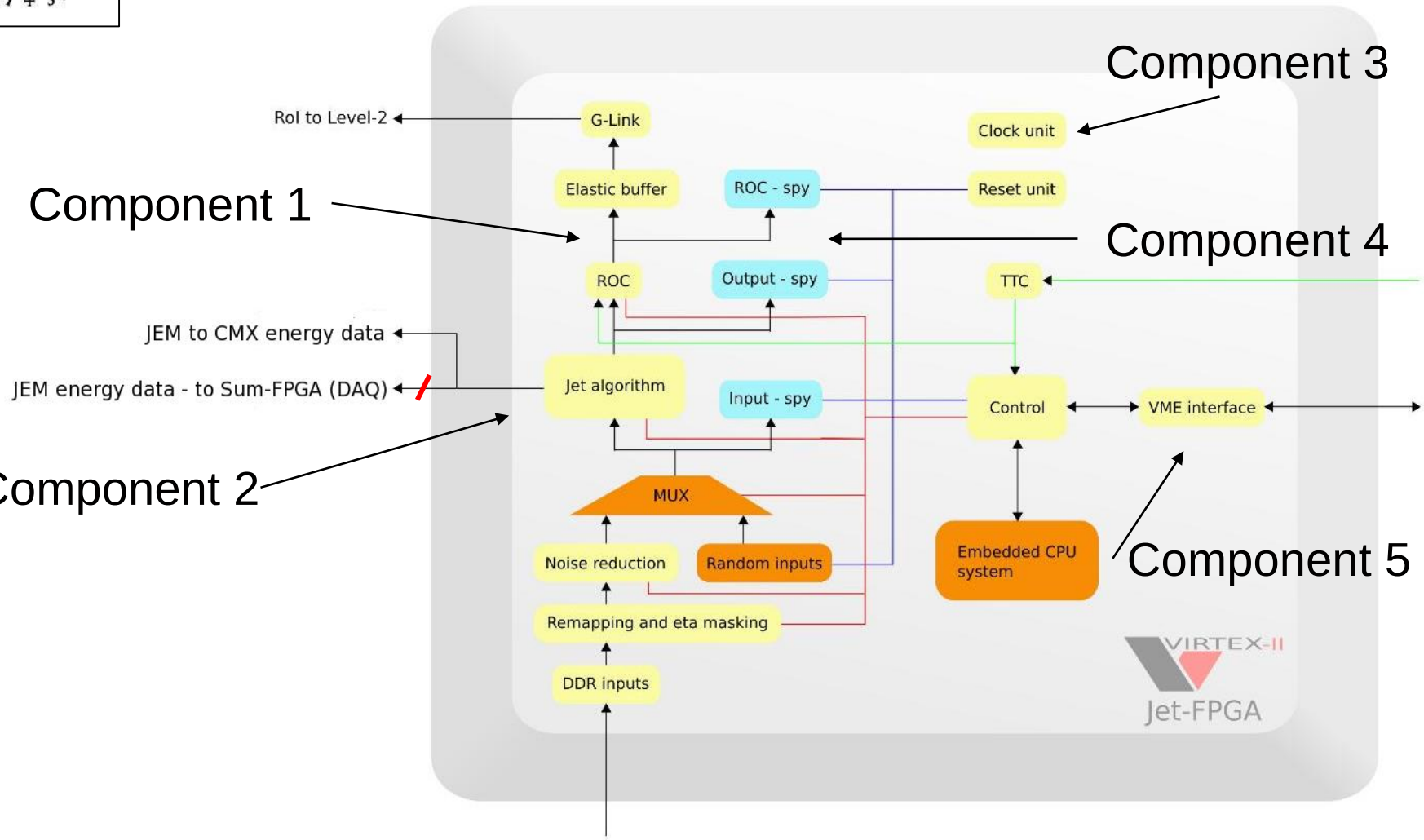
- Upgrade real-time path to 160 Mb/s backplane operation
- Route TOBs out of the backplane ports

- Affected components:
  - jet processor
  - energy sum processor

- In both processors update:
  - clock scheme
  - real-time &
  - non real-time data paths

Slides from
- Pawel: jet FPGA
- Uli: energy sum FPGA

Architecture of the jet-FPGA



Architecture is modular, its easier to add, replace or modify...

General remarks

- JEM-Jet firmware upgrade to add RoIs to the real time output.
- Algorithm will report up to four RoIs.
- 16 registers (thresholds), eta dependent thresholds easy to add.
- Updated components:

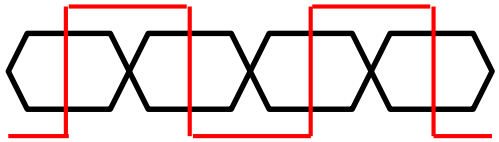
- Algorithm (including backplane@160MHz and DAQ data).
- VME interface.
- Glink stream (RoI-to-L2).
- SPY Memory.
- Clock manager (DCM, 160MHz).

- No design overhauls and no FPGA resource limitations to implement new functionality.
- Online software is updated (Jan, Duc, Murrough, Bruce).
- JEM-Jet firmware tests in progress at CERN (Pawel, Duc).

Energy sum FPGA

- Extract sum data before quad linear encoding
- Multiplex to 160Mb/s (160MHz clock)
- Calculate odd parity bit per sub-slice

- Generate phase shifted DDR clock on bit 24



- Playback/Spy memory on outputs probably not been used/supported for ages. Upgrade at all ?

- Single-bit readout stream into DAQ G-link to be updated.. no more jet data

Status/Plans

Jet FPGA firmware in good shape and tested

Sum FPGA firmware urgently to be modified and tested

- Required design software (ISE10.1) seems to be working again
- Hope to do code modifications in November
- Will do our best to provide at least a preliminary version for next test campaign

when ?