

JEP status

General → see Pawel

- JEP system (no recent tests with readout/ROIB)
- Jet FPGA firmware (ready)

Sum FPGA

- have been able to get the old ISE tools up again
- working on the firmware update right now
- readout format will be updated
- backplane energy sum format will be updated
- Re-work of RTDP and clocking scheme to 160MHz throughout
- Latency optimized version post M4
- expecting initial version ready for first tests at CERN in the week before M4
- integration with Pawel's diagnostics will have to wait until a later date