

Response to Comments

Tried to answer all questions that were received by 19:00, Jul. 30
Comments mainly fall into a few categories and can be answered globally:

- Typos, improvement on phrasing
 - Generally accepted, will be dealt with
- Request to add more details (textual description and drawings, including reference to gFEX)
 - Generally accepted, will be dealt with
- Technical details, in particular latency
 - Yes, will be added. Assume no major differences to eFEX figures, except:
 - PMA loopback latency is higher (1-1.5 BX estimate)
 - Parallel transmission latency figures (to neighbour FPGA) similar (tbc), but nowhere in the system PMA and parallel re-transmission are cascaded
 - Transmission to merger same figure
 - Regarding algorithms, expect to benefit from improved UltraScale performance

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- Component availability
 - Prototype using engineering silicon, in contact to distributor
- Questions about 12.8 Gb/s on inputs and outputs
 - 12.8 Gb/s operation has been verified in recent past on L1Topo prototype (Virtex-7 GTH, MiniPOD), even though focus has been on 6.4Gb/s operation
 - Extensive tests will take place well before jFEX prototype production, on L1Topo spare modules
 - Consider L1Topo a demonstrator for jFEX
 - jFEX prototype is basically more of the same, re-targeted to UltraScale
- Questions about impact of gFEX on jFEX capabilities
 - The overlap between jFEX and gFEX capabilities is intentional and has been judged as important to reduce risk for the phase 1 project. The gFEX endorsement includes a strong recommendation to pursue the full capabilities of the jFEX system at high link speeds