Who	Line	Comment	Response
Brawn	general	It would be good to see a picture of all the data links between FPGAs on a jFEX.	Agreed
Staley, Straessner & Qian	general	The Xilinx Ultrascale FPGAs. Do you have a 'road-map' or timescale for purchasing and using these FPGAs on a jFEX prototype? What is the expected delivery time scale once it is ordered? (From quickly looking on the Avnet and Xilinx web sites I can't see any devices or development kits/ eval-boards yet for sale.)	We are planning for engineering samples.Since we got confidential information only…
Staley	general	FPGA Configuration times. Do you have an estimate of how long configuration will take after power-on. Are the FPGAs configured sequentially, or together in parallel?	Final decision has not yet been taken. We try to come to a common solution with the eFEX.
Begel	general	The baseline precision from the LTDB is only 11 bits whereas the jFEX spec assumes 13 bits from LAr.	Available bit rates for input channels. Will be adjusted to the bit depth for each input module.
Straessner	general	Will the optical input plant and available connectivity on the jFEX be compatible with the future digital Tile readout in Phase-II? (more bandwidth?)	Due to the changes between Phase-I and Phase-II in the incoming Tile fibres, we would expect the optical input plant to be changed. The jFEX boards are designed to handle both situations. This might result in some spare links during Phase-I, due to the smaller energy bit count and BCMUX.
Straessner	general	ATCA: if I understand correctly, you foresee 6 x 10 Gb/s links per jFEX which are concentrated to one/two RODs: do plan to design a custom backplane or are there COTS backplanes which do the job?	Regular backplanes support 4 links per direction (incoming and outgoing). We plan to invert the direction of 2 of the incoming links to be able to use 6 x 10 Gb/s links to the ROD system.
Straessner	general	Interplay jFEX/gFEX: which of the functionality planned for the jFEX would be covered by the gFEX?	We have no detailed knowledge of the gFEX functionality. We will have to discuss this based on the gFEX specifications.
Brawn	103	This point needs clarifying. The links in the final system module will only work at one speed, but the prototype must be capable of supporting multiple speeds (as stated on line 129).	Agreed, will be modified in the next update of the document.

Who	Line	Comment	Response
Begel, Brawn & Schwienhorst	108	Section 3: The gFEX is now an approved component of the Upgrade L1Calo and so the figures and text should be updated to incorporate it. (See the ROD spec, in which these changes have been made already.)	will be done
Brawn	127	A more detailed explanation of the possible link speeds is needed here. (See comment to line 325).	Agreed
Schwienhorst	170	the optical plant also provides additional duplication not provided by sources.	Will be modified
Schwienhorst	218	should mention here different fiber contents depending on link speed?	Most changes in link speed have no effect on the covered region per fibre.

Who	Line	Comment	Response
Begel, Wells, Einsweiler & Henriques Correia	222	Is there an expectation that we'll need tau ID for |eta|>2.5 in Phase 2 if the ITK is extended to forward eta? If so, then how will this impact the current design? I can only say that Tau ID for eta>2.5 has been on our wishlist since the beginning of the TF in Feb, but no work has been done to the best of my knowledge. It would not be difficult to do some first studies with full calo sim and truth information for tracking, but no one is working on this. A priori, I think the case is not very strong, but as it is particularly interesting for example to look at the possibility of CP-mixing in H->tautau, as well as measuring spin/parity for A->tautau (since in many BSM Higgs models, the fermionic decays for the heavier neutral Higgs are more important than the bosonic ones, which are often suppressed), and much of the information about non-0+ spin-parity is carried at large cos(theta*), one could wish that there were both some performance and some physics results in this area. However, I would not expect anything until as a minimum, the Run1 H->tautau paper is out... So - it would not be possible to justify a request for large-eta triggering on taus at the present time. Since our experience so far is that tau triggers will always require two objects (lepton+tau_had, or tau_had+tau_had, or even large-MET+tau_had) to arrive at tolerable rates, then doing anything with taus beyond eta=2.5 probably does require triggering capability at large eta, but I could not expect anyone to want to invest more time in it without better justification than this EMail !	The algorithm will be modified to handle the coarser granularity but there is no impact on the hardware design. To be discueed
Schwienhorst	226	how many different algorithms will run in parallel? Do they only differ by window size? or also other parameters?	They will most likely also differ in other parameters like weighting. Studies for the determination of the exact algorithms are on-going.

Who	Line	Comment	Response
Brawn	230	Does the Tau algorithm use any isolation criteria? Is this an Rcore type algorithm?	At the current state the Tau algorithm has no explicit isolation criteria or Rcone condition. Only shower shapes are used by applying R-dependent weights.
Schwienhorst	246	is this paragraph still appropriate given that gFEX will happen?	The overlap between jFEX and gFEX capabilities is intentional and has been judged as important to reduce risk for the phase 1 project. The gFEX endorsement includes a strong recommendation to pursue the full capabilities of the jFEX system at high link speeds.
Brawn	258	Is anything known about the algorithms to operate at $32 < \|\eta\| < 4.9$?	Little. Might use some weighting to attribute energies to regular tower coordinates
Brawn	264	Event-by-event corrections of what?	Will be clarified
Begel	295	How much latency is required for the transmission of the environment via the low-latency links? (This is detailed in the eFEX technical specifications.)	???
Schwienhorst	299	- Fig 4: I don't understand the green towers. Are these still needed given that gFEX will happen? If they are still required, are these gTowers?	The 16 0.1 x 0.1 trigger towers are accompanied by two 0.2 x 0.2 cells, created by presumming four trigger towers.
Schwienhorst	299	- Fig 4 applies to the central jFEX modules. Please also provide an equivalent figure for the forward modules.	Agreed
Qian	299	Pg 10, Fig 4, my understanding from the previous text is that each processor FPGA receives optical links from DPS covering 2.8x1.6 (eta x phi). The diagram seems to indicate that each processor FPGA also receive direct optical links for the extended environment (green) area outside its core phi range. That would mean extra optical fan-out at DPS.	Each Processpr FPGA receives optical links from the DPS covering 2.4 x 1.6 (eta x phi) in fine granularity (0.1 x 0.1). The additional 0.2 x 0.2 cells do not require additional links sincy they use spare bandwidth of the existing fibres.
Brawn	312	Is this 40 links per Processor FPGA or 48 links in total? Also, you say at the end of this paragraph that the exact number of links required depends on the output bandwidth. Is 48 the upper limit?	48 links per Processor FPGA, can be increased if required

Who	Line	Comment	Response
Begel	316	Section 4.1.5: The assumption is 12.8 Gb/s communications between the jFEX and L1Topo. How does this change assuming the baseline 6.4 Gb/s?	There is no strict need to go down to 6.4Gb/s for the connection to the L1Topo even if the input bandwidth is reduced. The L1Topo has already successfully been tested at 12.8 Gb/s.
Brawn	325	Is this the first time 12.8 Gb/s is mentioned in the document? Given the mismatch between this and the baseline of 6.4 Gb/s cited in the TDR, I think a clearer statement on link speeds is needed earlier in the document, stating your aim is for 12.8 Gb/s, but you have fall-back positions for lower link speeds, down to 6.4 Gb/s.	Agreed
Brawn	349	Even though I proposed the concept of XTOBs, I'm not convinced they are of much benefit. In order to limit the bandwidth required for readout, I suggest we place a limit on the number of XTOBs that can be read out, in the same way we have with input data. Does it makes sense to use the same figure -- to limit them to 10% or the full L1A rate?	To be discussed
Brawn	390	The phrase "expects never to read out overlapping time frames" is ambiguous. Does it mean that functionality exists but is not expected to be used? Or does it mean that functionality does not exist?	Will be clarified
Brawn	403	Are these multi-Gb/s links in addtion to those described in 4.1.4? How many of them are there?	1 or 2 high-speed links from each Processor FPGA, in addition to the parallel links described in 4.1.4
Brawn	416	Previously we've said it should be possible to read out input data at a rate of 10% of the L0A, which is now 100 kHz, following the increase in the proposed L0A rate. Can we relax this requirement to 5% and so maintain the 50 kHz target? (The initial choice of 10% was arbitrary.)	To be discussed
Qian	426	2. Pg 14, Table 1. The trigger rate for XTOB is 500 KHz, and 1000 KHz for TOB. Why is this difference?	The XTOBs are nor necessarily required. The rate might be even lower than that.
Begel	429	Section 4.3: Please add the table of latency as per Sec. 4.3 of the eFEX technical specifications. I would appreciate additional entries for the transmission of information between the processing and merging FPGA.	Table will be added. There is no reason to assume any difference to the eFEX in terms of latency at data transmission to the Merger.

Who	Line	Comment	Response
Straessner	451	TTC distribution via ATCA backplane: do you expect latency issues?	We are under pressure to stay in our latency budget. However we do not see any problems coming from the TTC distribution in terms of latency.
Straessner	510	* Mapping of LAr input channels (I should probably know, but maybe you can explain again): Section 5.1.1: I understand that in a 0.4x0.4 central area you have 16 0.1x0.1 towers. But which are the 2 additional 0.2x0.2 towers? Are these some remaining towers from the 2.4<eta<3.2 area in the same phi region? Section 5.1: When I count the number of 0.2x0.2 towers in 2.4<eta<3.2 and phi of 0.4, I get only 8 towers and not 12, which would go on 1 fiber. What am I doing wrong?	The additional 0.2x0.2 towers are pre-summed 0.1x0.1 towers. They origin from the same phi region, but within |eta|<2.4. The 0.1x0.1 granularity is available in the region with |eta|<2.5. This first eta bin gives the additional 4 towers.
Qian	511	3. Pg16, Sec 5.1 para 1. Some diagrams are needed here. It is hard to follow the numbers without diagrams.	Agreed
Schwienhorst	521	I understand that you assume an input link speed of 12.8 Gb/s, but it would be very useful to also specify what formats would be for a rate of 6.4 Gb/s.	For 6.4Gb/s the input per fibre is reduced to 8 towers.
Begel	530	Section 5.1.1: What is the reasoning behind the choice of 13 bits for all ET quantities? (I couldn't find a justification in the TDR.)	Available bit rates for input channels. Will be adjusted to the bit depth for each input module.
Qian	530	4. Pg17, Sec 5.1.1. What useful data formats could possibly be for lower link speeds, say 9.6Gbps? Does the current jFEX design preclude the lower link speed options completely from physics point of view?	All (resonable) link speeds between 9.6Gb/s and 12.8Gb/s are suitable for the current jFEX design. Data formats for lower speeds will be included.

Who	Line	Comment	Response
Begel	538	You are assuming the calorimeter will use 12.8 Gb/s links. If the calorimeter runs at the 6.4 Gb/s baseline then the available payload is only 128 bits per bunch (including the 8b CRC). This implies a significant decrease in the available ET resolution and/or range. What are the implications?	see 521
Begel	553	There are a maximum of 24 TOBs at 12.8 Gb/s (with many fewer if the links run at the 6.4 Gb/s baseline). How are the TOBs distributed between the narrow jets, large jets, and taus? What are the maximum number of TOBs for each algorithm? How will these be prioritized? (Note that most taus will almost certainly also produce narrow-jet TOB and possibly large-jet TOB unless overlap removal is implemented within the jFEX.)	The best use of the limited number of TOBs as well as possible suppression of overlapping TOBs will require detailed studies.
Begel	567	Figure 7: 15 bit ET is used for the large-R jet TOB. Why does this require a larger dynamic range and/or precision than the narrow-jet TOBs which are only 13 bits?	Can be reduced if more bits are required for other information.
Schwienhorst	602	Presumably this count should be updated given that there will be a gFEX.	No, same numerology (spare bandwidth)
Schwienhorst	602	- What about spare fibers? Where are they and where are they routed?	For the prototype all spare fibres will be routed to the backplane.
Schwienhorst	605	is space available to have more than four MTP connectors? The eFEX utilizes 4 ribbons per cable (i.e. 48 fibers). Is it possible for the jFEX to go to five input connectors with four ribbons per connector?	Not impossible but very incovinient.
Brawn & Qian	614	“All of the signals received from the calorimeters are transmitted to two Processor FPGAs.” It should be four Processor FPGAs, right? Or is this sentence intended to mean that each of the received signals is transmitted to two of the four Processor FPGAs?	Each of the signals is transmitted to two of the four Processor FPGAs. This will be clarified in the text.

Who	Line	Comment	Response
Begel	654	While the XCVU190 looks like a very nice FPGA, it is unlikely to be available on the timescale of the prototypes for Fall 2015. (I only see the 080 & 095 on Avnet and those are listed as "non-physical inventory.") What is the fall-back solution for the prototype tests? Given that the package size of the XCVU190 is 50x50 doesn't this also require also require an additional prototype cycle?	Engineering silicon will be used on the prototype. We are already in contact with our FPGA distributor.
Straessner	654	Xilinx XCVU190: do you have an estimate if the resources are sufficient for the many functionalities and large coverage that you like to implement? do you have maybe some example implementations which can be scaled to the full version (e.g. sliding window for different areas/jet sizes, pile-up corrections, etc)?	We made an estimate on the required resources for the planned algorithms for gFEX hardware panel some months ago. We came to the conclusion, that the logic resources should be sufficient, even though this estimate was based on a smaller FPGA (XCVU160).
Brawn	660	This is the first use of the term "pile-up sums". Line 630 names "additional data". Pile-up sums and their use should be described in section 4.1.2 (algorithms).	Agreed
Qian	731	6. Pg.24 Sec 6.4. So the clocking design on jFEX will support several link speed options, namely 6.4G/9.6G/11.2G/12.8G, right?	Yes, the prototype will support a wide range of link speeds.
Brawn	760	What PCB simulation tool are you planning to use? We should co-ordinate if possible.	So far considering Hyperlynx
Brawn	761	For the eFEX, we have abandonned our attempts to extract the System ACE IP from Xilinx. We are now planning a simple Master SPI configuration scheme, the details of which we are happy to share.	We should opt for a common approach. Considering small configuration mezzanine for improved flexibility
Qian	761	7. Pg 25, Sec 6.6. Could you get hold of the Xilinx System ACE SD Controller IP?	We should opt for a common approach. Considering small configuration mezzanine for improved flexibility

Who	Line	Comment	Response
Straessner	810	Is the cooling power of an ordinary ATCA shelf sufficient? Could there be problems if the cooling blocks of the 2 x 2 FPGA arrangement cover each other's air flow?	Our current estimate on the power consumption is about 50W per Processor FPGA. Modern ATCA shelves support cooling of up to 450W per slot. This leaves sufficient cooling capacity for the remaining parts of the boards. The impact for on cooling will be considered during the designing phase of the PCB.
Begel, Brawn & Qian	810	Section 6.8: What is the expected power utilization of each jFEX board?	~300-350W for per module
Straessner	878	MPO zone 3 connectors to RTM: did you already make some tests of the connection/disconnection? Is this robust (i.e. anyone can insert the boards and it works) or delicate?	This is currently being tested on the L1Topo.
Straessner	935	* Board layout (for my curiosity): did you consider also a solution with processing FPGAs on AMC mezzanine cards (like LAr LDPS)? If so, what was the reason to go for an all-on-1-board solution?	The Processor FPGAs require a huge bandwidth for communication between each other and with the Merger FPGA. The required number of pins is more than the available pins on an AMC connector.
Brawn	936	This looks suspiscously like the eFEX…. Is this really your layout?	Represents the jFEX, a more detailed version will follow
Brawn	117	Remove comma after "does this".	Agreed
Brawn	214	Should read "data *are* ".	Agreed
Brawn	268	A diagram showning the area processed by one jFEX (in the central region), the different areas of granularity, and how this space is divided between the FPGAs would be good.	Agreed
Brawn	291	Should read "data are".	Agreed
Brawn	426	It would be useful if this table also showed the bandwidth per backplane link to the ROD.	Agreed
Brawn	595	Is this a different font size?	Yes, will be adjusted.
Brawn	613	Space before comma should be removed.	Agreed

Who	Line	Comment	Response
Brawn	614	To me, this sentence makes it sound as if two Processor FPGAs receive all the input data, and therefore two receive nothing. I suggest you reword it something like "each of the received signals is transmitted to two of the four Processor FPGAs.	Agreed
Brawn	811	Is this a different font size?	Yes, will be adjusted.