L1Topo PCB/assembly saga

Prototype

- PCB production at company **W**
- 20 working days starting on — 11.04.2013
  - delay — 13.05. --> 24.05.2013
  - delay — 24.05. --> 04.06.2013
- assembly at company **S** — 06.2013
- lab test Mainz — 07.2013
  - JTAG Boundary Scan errors found…
- assembly 2nd copy prototype at ProDesign
  - trying… — 01.2014
  - micro vias not filled properly/uneven surface ! (explains issues with 1st copy)
  - new PCB round **W,** 30 working days — 01.2014
  - PCB delivery — 03.2014
  - assembly at ProDesign <1wk — 03.2014
  - delivery — 03.2014
  - JTAG Boundary scan ok — 03.2014 → prototype successfully built !

Production module (ProDesign + **X** (PCB))

- order out to ProDesign — 09.2014
- PCB delaminated during assembly — 11.2014
- baking PCB (spare) tested ok — 11.2014
- 2nd copy assembled/delaminated — 11.2014
- redo PCBs — 11.2014
- assembly last week — 12.2014
- delivery 1st copy — today, looks good, initial results next wk.