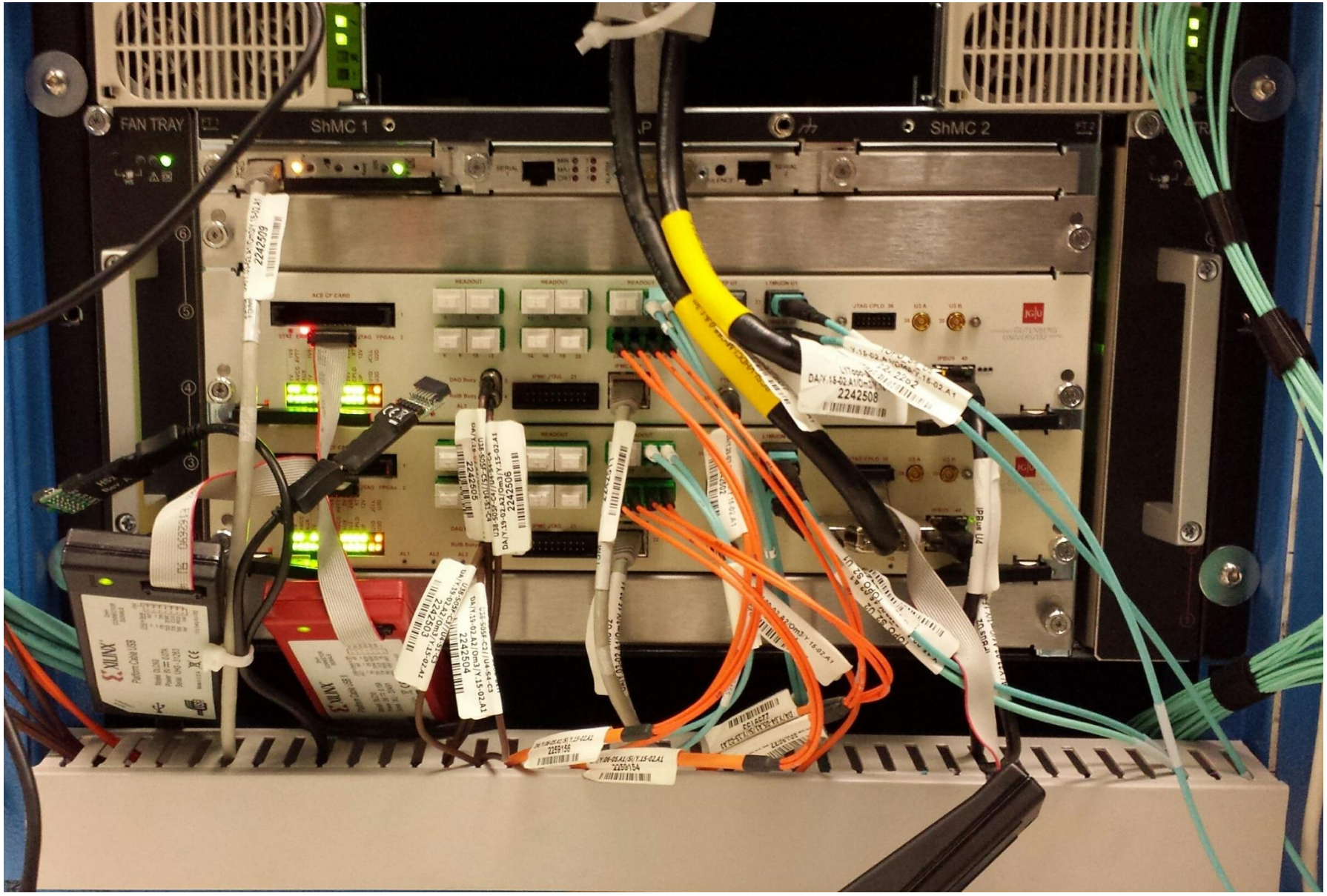
L*Topo

Run-2 → Phase-1 → Phase-2

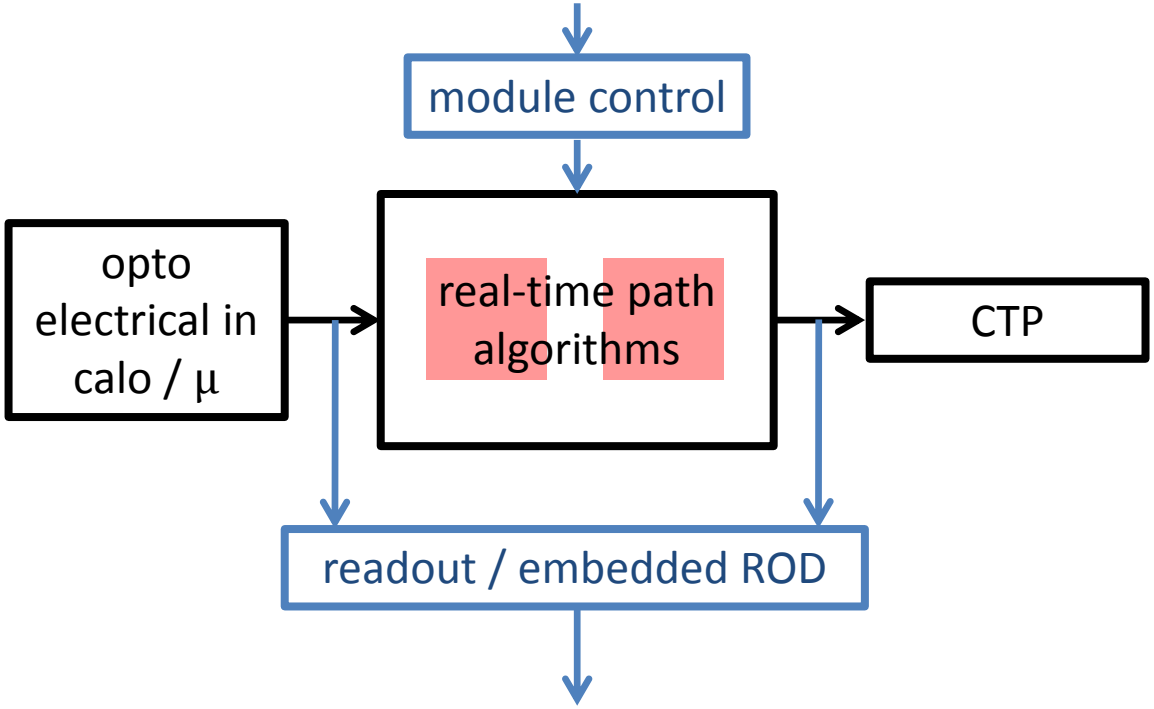
Uli / Mainz

L1Topo in its habitat



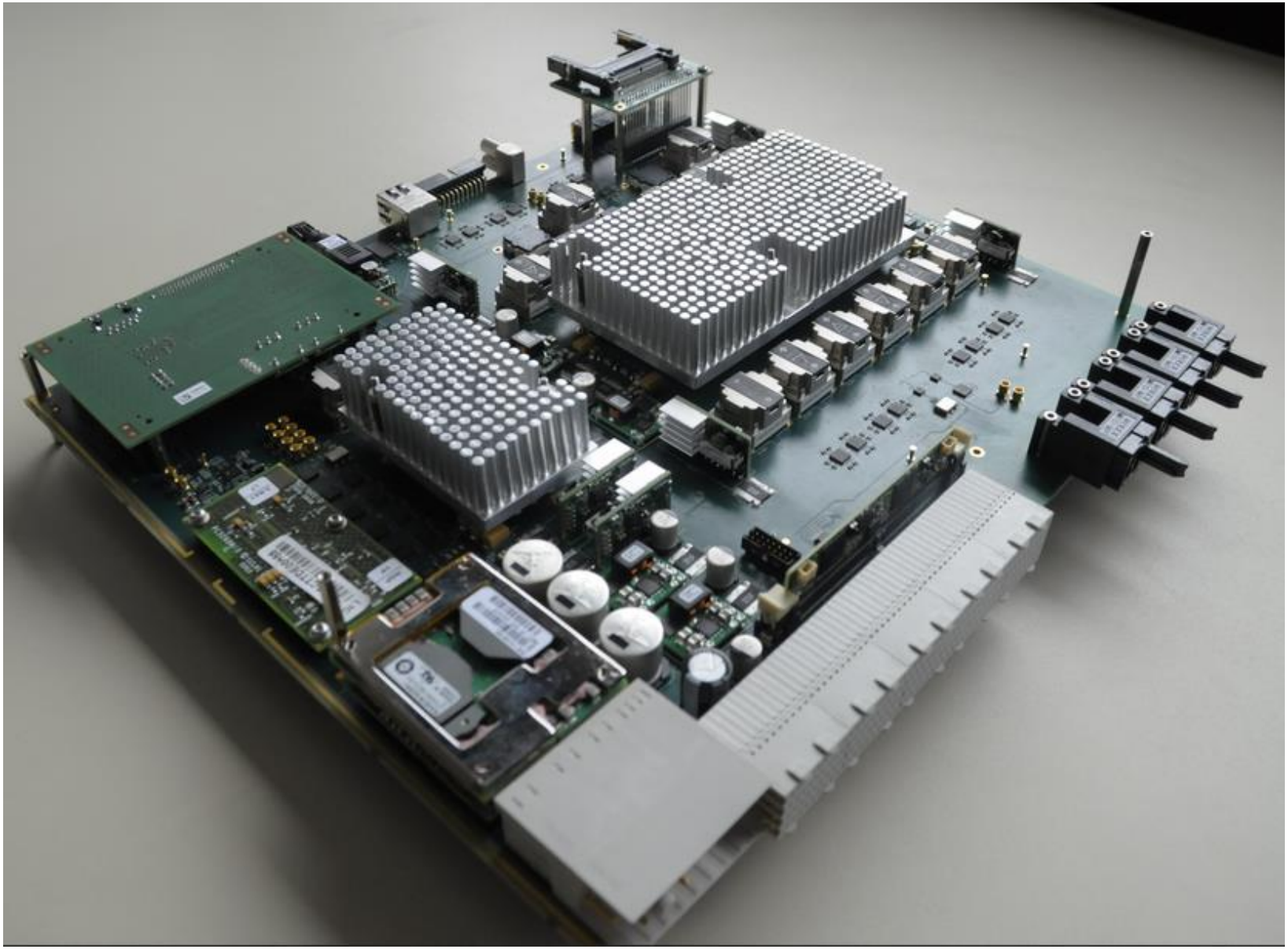
L1Topo / run 2

L1Topo / Run-2

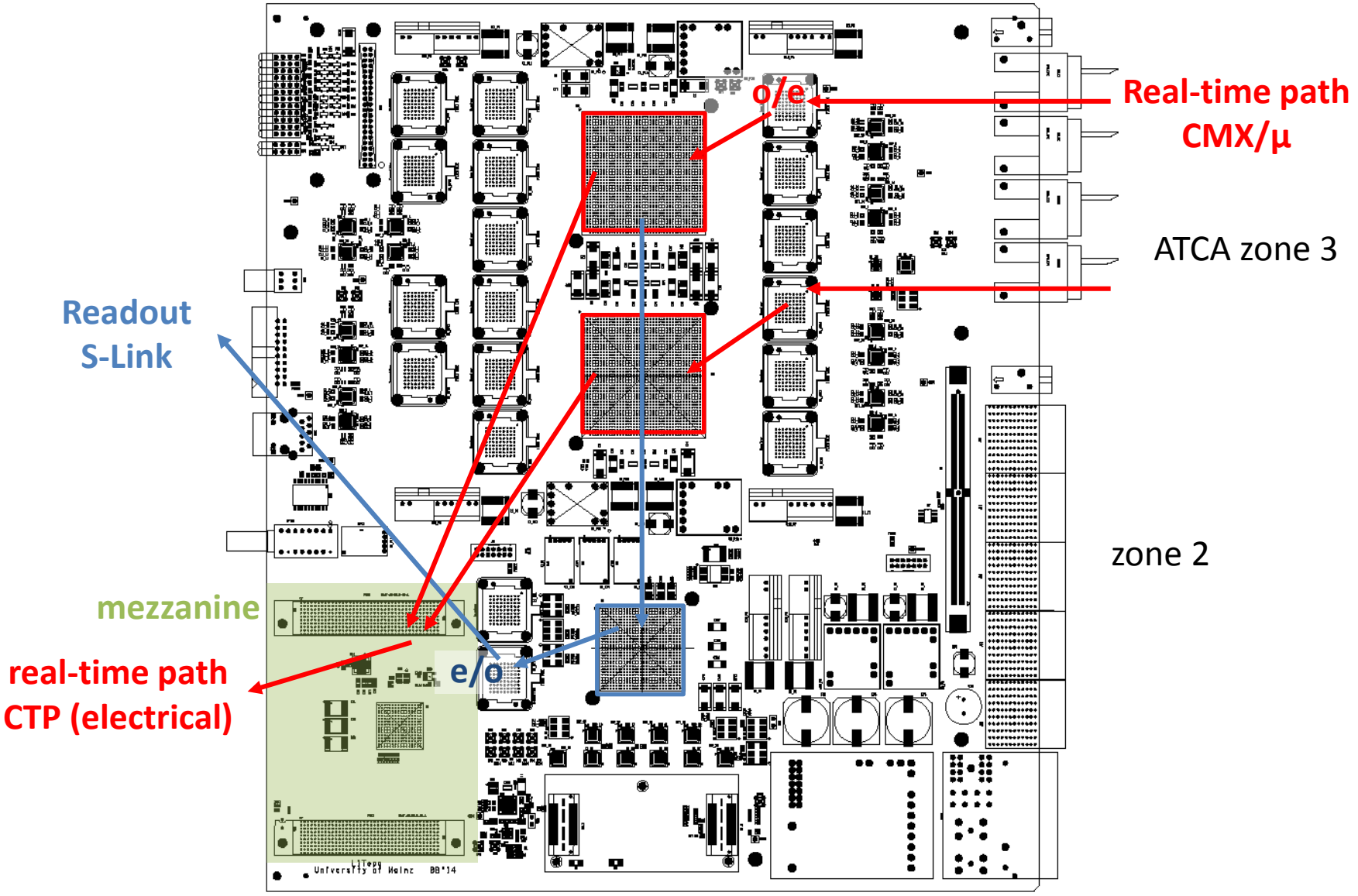


- five modules built for run 2
  - two algorithmic processors
  - one DAQ/control FPGA
  - designed for phase-1/phase-2 compatibility
- two modules deployed at point 1

L1Topo unplugged



L1Topo floor plan / run-2

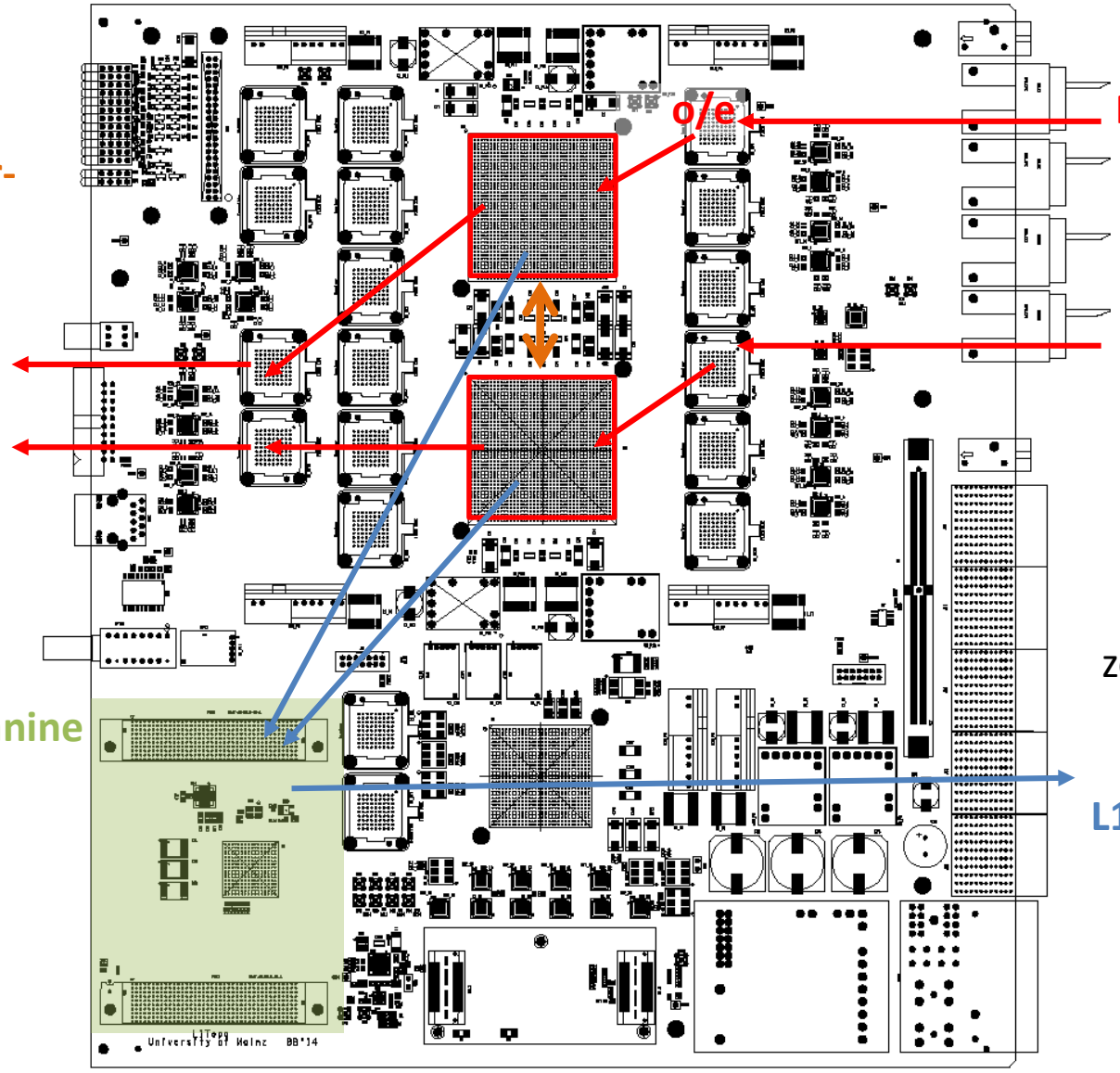


L1Topo → phase 1

- New L1Topo production for phase 1
- 3 new modules were initially planned for phase 1
  - 2 × topology
  - 1 × hit merger for L1Calo multiplicity triggers
- Current L1Topo can act as a prototype:
  - Existent modules expected match needs for Phase-1
  - No changes to concept
  - Will need to run new PCB production anyway
  - Will allow for improvements / adaptation to upcoming phase-2 requirements

- Expected to live in an ATCA water cooled "standard" shelf
  - Space
  - Power / cooling

L1Topo floor plan / phase-1



Summary: Modifications wrt run-2

- Connect to L1Calo hub/ROD modules via backplane
  - Requires different extension mezzanine
  - Basically route-through of 16 high-speed signals
  - DAQ/ROI
  - Clock / TTC data
- Switch-on inter-processor communication
  - Signals duplicated between FPGAs rather than forward duplication upstream
  - Adds bandwidth for incoming signals
  - Latency: be prepared to continue duplicating a fraction of signals upstream. The ones on latency critical path…
- Add output bandwidth for signals into CTP
  - Optical link
  - No plan to remove electrical link (latency ?)
- One possible modification under consideration already now:
  - We might prefer the CERN recommended jitter cleaner (used on jFEX prototype) over the one used on L1Topo

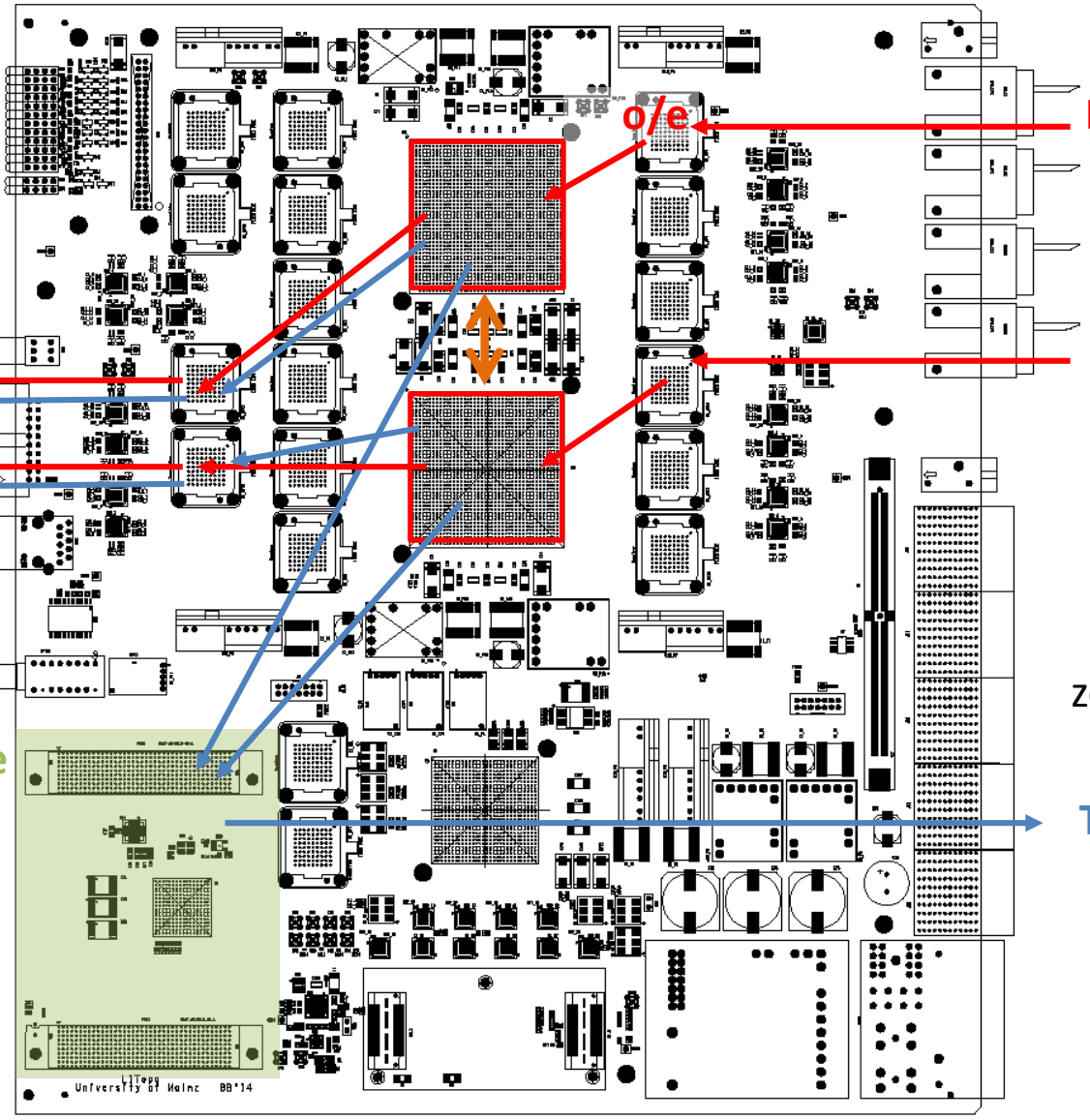
Needs / changes for phase-2

… as known by now

- Challenging processing: more/complex algorithms
- Fortunately less stringent latency requirements
- Far less duplication of resources required
- Time multiplexing might be possible

- Plus the need to supply ROIs to "Regional Readout Request" (R3) logic
  - Near real-time
  - Latency approximately on the same scale as L0 trigger
  - Will not be possible through the backplane / L*Calo hub/ROD modules
  - ROIs basically TOBs that fired topo algorithms
  - *… how many ?*

L0Topo floor plan / phase-2



Summary of changes for phase-2

- Optical output bandwidth needs to be shared between L0 and R3 data
  - Total bandwidth available per module : 24 * ~10Gb/s
- Algorithmic firmware will need to be modified to address
  - Need for complex algorithms
  - Need to identify TOBs that fired the triggers
  - Involves tagging / pipelining the TOBs such that at time of decision the information is still available
  - Route the TOBs / ROIs out to high-speed links

In the light of two well-filled L1Topo modules in run-2:

- The system is scalable
  - Standard ATCA crate has 12 slots available for processor blades
  - Will allow for additional modules to be installed

Summary / outlook / discussion

- The L1Topo module concept will allow smooth transition run-2 / phase-1 / phase-2
- Hardware modifications will be possible
- System is scalable, larger module count not ruled out
- Upstream modules should allow for sufficient output bandwidth
- Bandwidth for ROI data of ~200Gb/s per module probably adequate ?
- If not: need to understand now
- Spare output bandwidth on processor FPGAs available
- Need to be routed out to additional opto/electrical converters

- Firmware will require major changes to benefit from increased latency and to support R3 concept