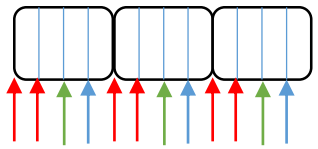
Post automatic fine delay : two data/clock phases illegal (**red**), since after next re-configuration data might have moved by +/- one sub-tick wrt global clock and we would have moved data into next /previous BX



Data eye out of de-serializer, valid for four sub-ticks

Global clock, four different options pre manual fine delay

In case we see data/clock phase shown in **red** we will have to add a delay of 1 or 2 subticks from the data base