

# jFEX and L1Topo module control

- L1Topo and jFEX are modular devices
  - 2/4 instances of processor + opto transceiver on board
  - Module control mainly on mezzanines
- jFEX prototype in production (almost done)
- Decision on L1Topo/Phase-1 asap. Need requirements and clear statement from community
- Prototype either
  - Current L1Topo/0 or
  - Current jFEX (production module will be synthesis of both)
- jFEX has **all** control functionality located on mezzanines
- L1Topo/0 has control FPGA on board (eROD,IPbus), but requires some mezzanine rework for Phase-1 anyway.
- Aiming at a consistent control scheme for both modules at phase-1
  - Module control / IPbus
  - FPGA configuration
  - Extended environmental monitoring / I2C
  - (clock synthesis / jitter reduction)

# L1Topo/jFEX module control history

- L1Topo/0
  - Standard IPbus
  - SystemACE FPGA configuration
  - Environmental monitoring / I2C via control FPGA (Kintex)
  - No embedded controller
- jFEX initially planned for FPGA based control
- Started considering change to Zynq based scheme
  - Rouven S. has been working on required hardware and software (PetaLinux)
  - PicoZed (7030) daughter card on jFEX extension mezzanine
  - Required connectivity for control, I2C, configuration, clocking
  - Rouven not with our group anymore, lacking Zynq specific effort now
- Use programmable logic resources within Zynq (Artix) only for monitoring, control and configuration.

# Plans

- Follow both options (FPGA vs. Embedded controller) at conceptual level for a little while
- Live with FPGA-only until further effort on the horizon
- Probably base final decision on whether Zynq officially supported in ATLAS DAQ world.
- Final decision can be taken at a rather late stage since relatively simple mezzanine. Mainboard not affected. Zynq based scheme might be somewhat more expensive than simple FPGA scheme...

... have to limit effort in control area since busy with real-time stuff...