# Hardware trigger processor demonstrator

L1Global demonstrator presented at June joint meeting

Now going into detailed design phase

- Modular design
- Base board probably ATCA compliant
- Explore ALTERA high performance / high bandwidth FPGAs
  - Start with what's available now: Arria10
  - Move on to pin compatible Stratix10 as it comes to the market: 28Gb/s
  - Move on to 56Gb/s PAM-4

Finding appropriate optoelectrical transceivers might be challenge

- Allow for choice of opto devices by defining daughter module reference pinout
- Current favourite: use a couple of Samtec FireFly sockets with defined relative position

  → mount two FireFly modules

  → mount custom carrier for alternative product (up to 24x)

# demonstrator

- Eventually we expect to have a module available with one control FPGA, two high-performance/high bandwidth processors and associated opto fibre connectivity
- We are planning to route additional high-speed links onto a mezzanine socket, allowing for connection to an auxiliary processor (eg. GPU via PCIe), should that turn out to be advantageous.

- Note: it seems Altera is aiming to get a large variety of heterogeneous multi-chip packages onto the market over the next couple of years. The demonstrator will be built such as to exploit capabilities of further upcoming devices (eg. high memory count devices) if we consider them beneficial for trigger processing purpose.

# demonstrator

- Starting as technology demonstrator
  - Next generation FPGAs
  - Opto transceivers
  - PAM-4 encoding
  - (GPU optional)
- Turn it into functional demonstrator once required functionality becomes clearer
- Test bed for firmware development