L1Topo for Phase-1

jFEX prototype currently under production. Highly **modular** design. Equipped with large UltraScale and Ultrascale+ devices.

- Expect completion next week
  - standalone tests in home lab in November
  - Initial CERN tests just before Christmas if things going smoothly
- jFEX prototype can be turned L1Topo replacement by some mods along the lines of current L1Topo. Need Topo style mezzanine plus:
- Fork the design:
  - jFEX with 4 FPGAs for maximum data duplication
  - L1Topo with 2 FPGAs for minimum latency and cost reduction. Output and electrical connectivity modified as for current L1Topo

  → Plan "B"

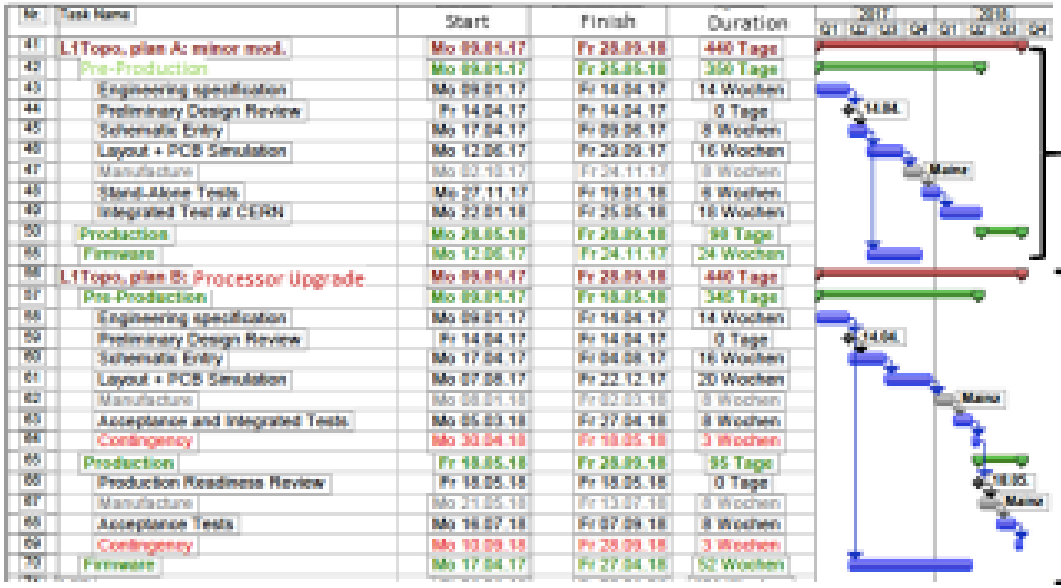
Current L1Topo can be made phase-1 compatible (standard L1Calo ROD/TTC interface)

- Replace mezzanine
- Verify inter-FPGA parallel link operation, qualify max. bandwidth/latency, verify ATCA fabric interfaces
- Replace configurator module (SystemACE based)

  → Plan "A"

Introduction

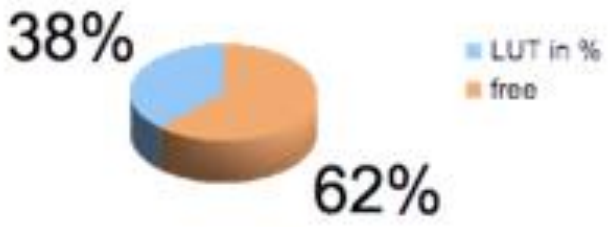
- Two possible L1Topo designs for Phase1:
  - Plan A: Minor modifications of Phase0 Topo
    - New mezzanine module for compatibility with ROD/TTC Phase1 design
    - Two additional miniPOD devices to double output bandwidth
  - Plan B: Processor upgrade (For details see following slides)



Topo Design	RT in	RT out	ROI engine out	Readout Path
Plan A	160 Links @ 11.2 (12.8) Gb/s	4 Links @ 12.8 Gb/s	44 Links @ 12.8 Gb/s	12 Links @ 6.4 Gb/s
Plan B	240 Links @ 11.2 (12.8) Gb/s	4 Links @ 12.8 Gb/s	44 (92) Links @ 12.8 Gb/s	12 Links @ 6.4 Gb/s

Resource Usage of Phase0 Topo

M00U1



M00U2

74% 2017 menu ???

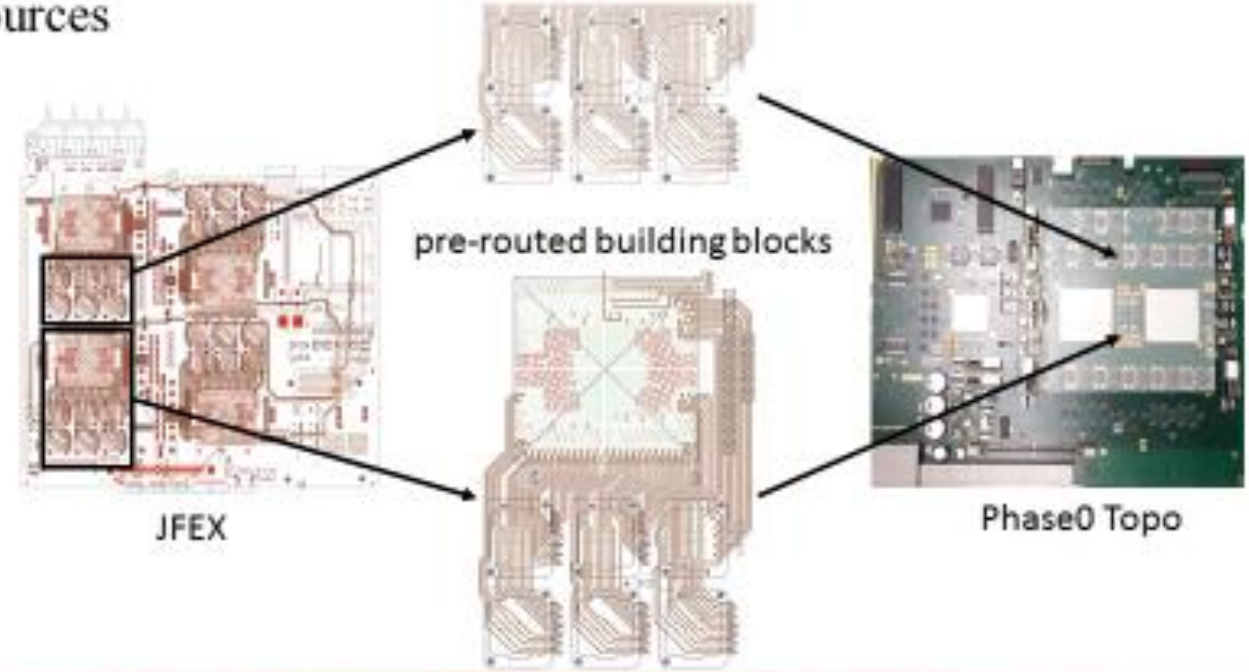
M01U2

M01U2

- Phase0 Topo already at its limit
- Not much flexibility for adding new and more complex algorithms

Plan B – Processor Upgrade

- Goal: more powerful FPGAs and maximum input/output bandwidth
- Phase0 Topo and current jFEX prototype use a modular design (mezzanine, pre-routed building blocks, …)
- Combine existing jFEX building blocks with Phase0 Topo design (replacing XC7VX690T device), only small re-routing required
- Gain 40 MGT links per device, plus considerable amount of logic and memory resources



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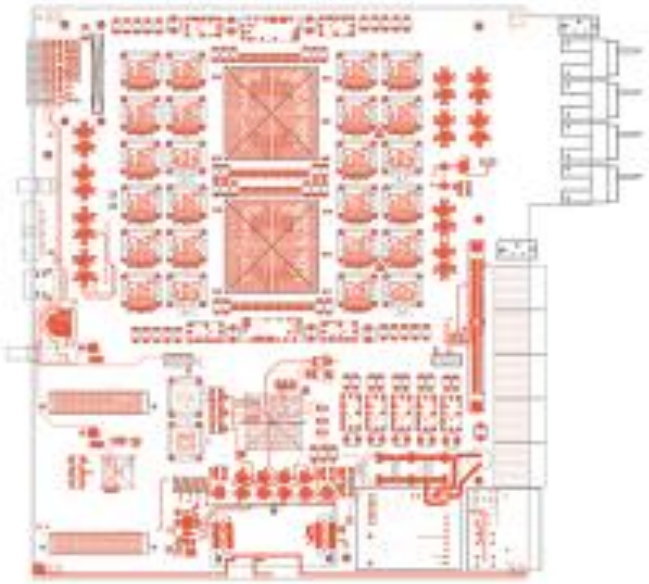

Summary

- FPGA:
  - Plan A:
    - XC7VX690T (Virtex 7), logical cells: 693120, 18Kb RAM blocks: 2940 (Utilization 81%)
  - Plan B:
    - XCVU190 (Virtex UltraScale), logical cells: 2350000 (factor of ~3 more resources) , 18Kb RAM blocks: 7560 (Utilization 35%)

- Bandwidth:

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(My very personal) conclusion

- We might well be short of resources on current L1Topo soon, if requests for menu changes continue to come in
- Latency might be an issue on current module due to likely requirement of inter-FPGA links at phase-1.

→

- Urgently start with jFEX based design work
  - Specs now
  - Schematics to start asap
- Make sure that this more advanced, higher performance module is considered baseline → fall-back to older design always possible
- At L1calo joint meeting support for this option
- Early decision in this direction will allow for contingency in schedule