JOHANNES GUTENBERG UNIVERSITÄT MAINZ

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ATLAS EXPERIMENT http://atlas.ch

Topo Phase1

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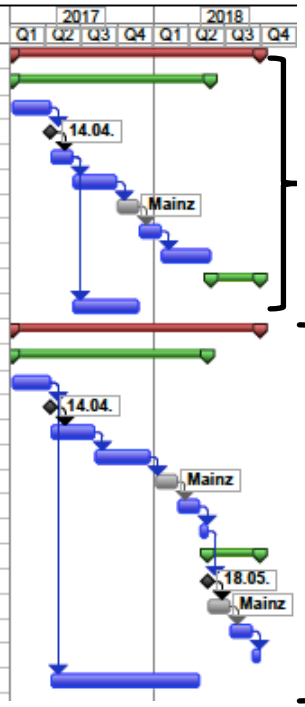
Introduction

- Two possible L1Topo designs for Phase1:
  - Plan A: Minor modifications of Phase0 Topo
    - New mezzanine module for compatibility with ROD/TTC Phase1 design
    - Two additional miniPOD devices to double output bandwidth
  - Plan B: Processor upgrade (For details see following slides)

Nr.	Task Name	Start	Finish	Duration
41	L1Topo, plan A: minor mod.	Mo 09.01.17	Fr 28.09.18	440 Tage
42	Pre-Production	Mo 09.01.17	Fr 25.05.18	350 Tage
43	Engineering specification	Mo 09.01.17	Fr 14.04.17	14 Wochen
44	Preliminary Design Review	Fr 14.04.17	Fr 14.04.17	0 Tage
45	Schematic Entry	Mo 17.04.17	Fr 09.06.17	8 Wochen
46	Layout + PCB Simulation	Mo 12.06.17	Fr 29.09.17	16 Wochen
47	Manufacture	Mo 02.10.17	Fr 24.11.17	8 Wochen
48	Stand-Alone Tests	Mo 27.11.17	Fr 19.01.18	6 Wochen
49	Integrated Test at CERN	Mo 22.01.18	Fr 25.05.18	18 Wochen
50	Production	Mo 28.05.18	Fr 28.09.18	90 Tage
55	Firmware	Mo 12.06.17	Fr 24.11.17	24 Wochen
56	L1Topo, plan B: Processor Upgrade	Mo 09.01.17	Fr 28.09.18	440 Tage
57	Pre-Production	Mo 09.01.17	Fr 18.05.18	345 Tage
58	Engineering specification	Mo 09.01.17	Fr 14.04.17	14 Wochen
59	Preliminary Design Review	Fr 14.04.17	Fr 14.04.17	0 Tage
60	Schematic Entry	Mo 17.04.17	Fr 04.08.17	16 Wochen
61	Layout + PCB Simulation	Mo 07.08.17	Fr 22.12.17	20 Wochen
62	Manufacture	Mo 08.01.18	Fr 02.03.18	8 Wochen
63	Acceptance and Integrated Tests	Mo 05.03.18	Fr 27.04.18	8 Wochen
64	Contingency	Mo 30.04.18	Fr 18.05.18	3 Wochen
65	Production	Fr 18.05.18	Fr 28.09.18	95 Tage
66	Production Readiness Review	Fr 18.05.18	Fr 18.05.18	0 Tage
67	Manufacture	Mo 21.05.18	Fr 13.07.18	8 Wochen
68	Acceptance Tests	Mo 16.07.18	Fr 07.09.18	8 Wochen
69	Contingency	Mo 10.09.18	Fr 28.09.18	3 Wochen
70	Firmware	Mo 17.04.17	Fr 27.04.18	52 Wochen

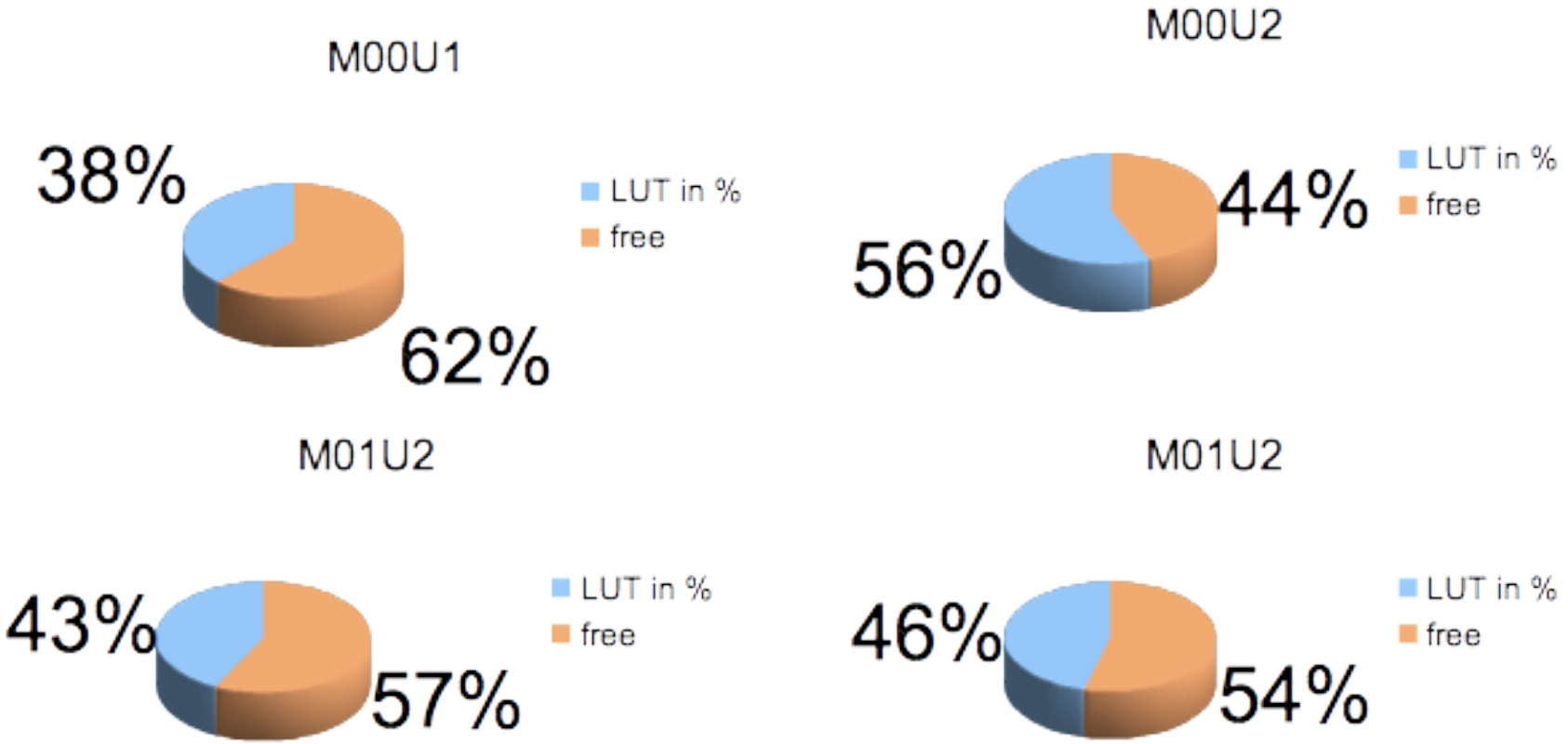


Plan A
Schematic Entry + Layout:
24 weeks

Plan B
Schematic Entry + Layout:
36 weeks

Topo Design	RT in	RT out	ROI engine out	Readout Path
Plan A	160 Links @ 11.2 (12.8) Gb/s	4 Links @ 12.8 Gb/s	44 Links @ 12.8 Gb/s	12 Links @ 6.4 Gb/s
Plan B	240 Links @ 11.2 (12.8) Gb/s	4 Links @ 12.8 Gb/s	44 (92) Links @ 12.8 Gb/s	12 Links @ 6.4 Gb/s

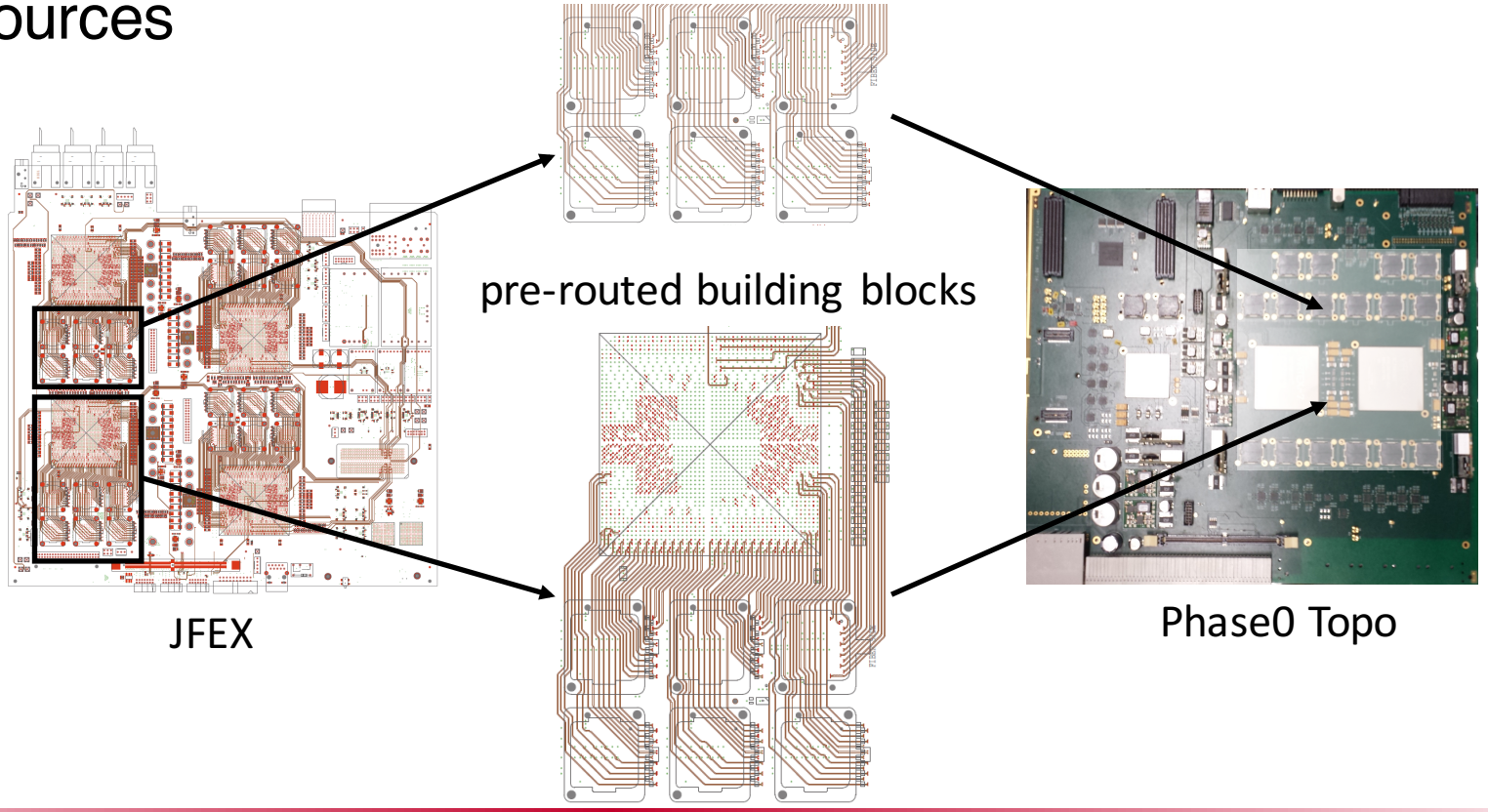
Resource Usage of Phase0 Topo



- Phase0 Topo already at its limit
- Not much flexibility for adding new and more complex algorithms

Plan B – Processor Upgrade

- Goal: more powerful FPGAs and maximum input/output bandwidth
- Phase0 Topo and current jFEX prototype use a modular design (mezzanine, pre-routed building blocks, …)
- Combine existing jFEX building blocks with Phase0 Topo design (replacing XC7VX690T device), only small re-routing required
- Gain 40 MGT links per device, plus considerable amount of logic and memory resources



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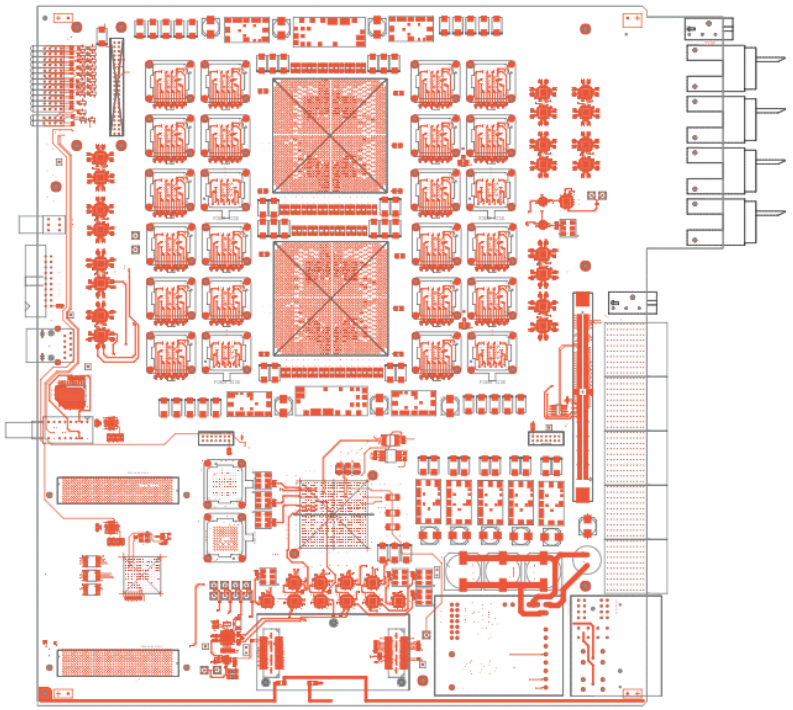

Summary

- FPGA:
  - Plan A:
    - XC7VX690T (Virtex 7), logical cells: 693120, 18Kb RAM blocks: 2940 (Utilization 81%)
  - Plan B:
    - XCVU190 (Virtex UltraScale), logical cells: 2350000 (factor of ~3 more resources) , 18Kb RAM blocks: 7560 (Utilization 35%)

- Bandwidth:

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