DCS on jFEX and L1Topo in Phase-1

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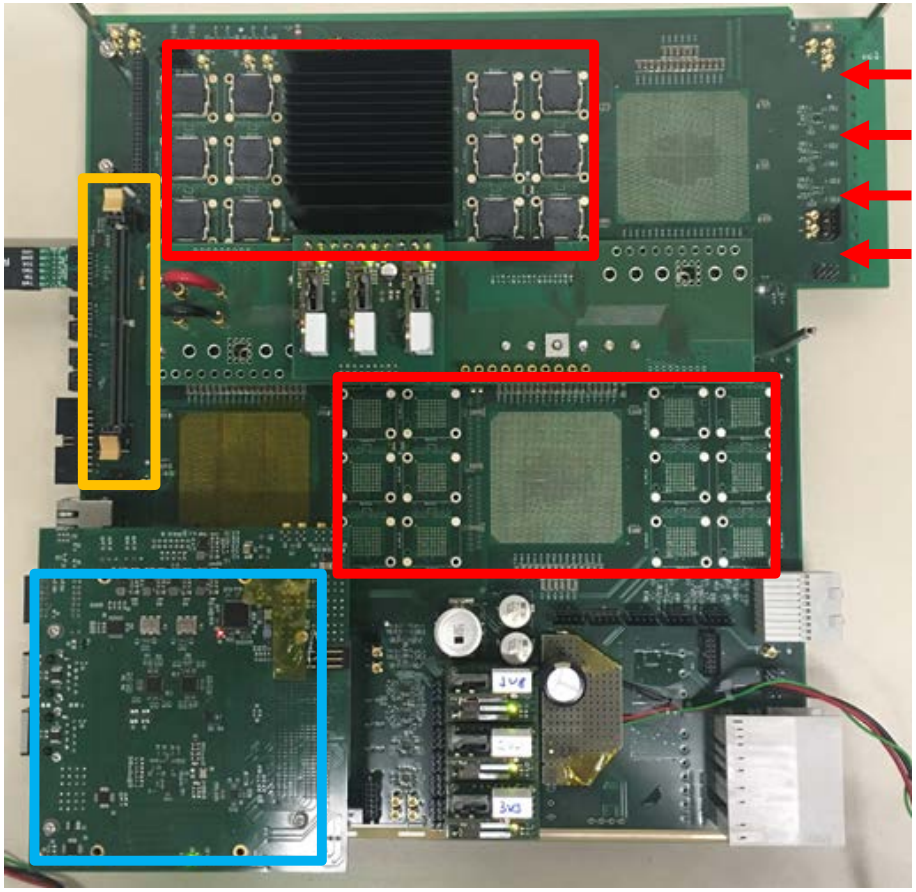
Pre-history: Topo in Phase-0

- LAPP **IPMC** available on L1Topo
  - Initial firmware work done by Adam
  - Readout of all sensors, handle switch, power negotiation
  - Not currently in use
- Additional data available
  - Some environmental data collected by control and processor FPGAs
    - Direct FPGA-internal sensing of temperatures and voltages
  - Some devices controlled and monitored by I2C (opto devices, clock conditioners,...)
  - Sub-set of these data can be sent into DCS via **IPbus**/OPC server

L1Topo / jFEX @ Phase-1

New **L1Topo** based on **jFEX** mainboard with

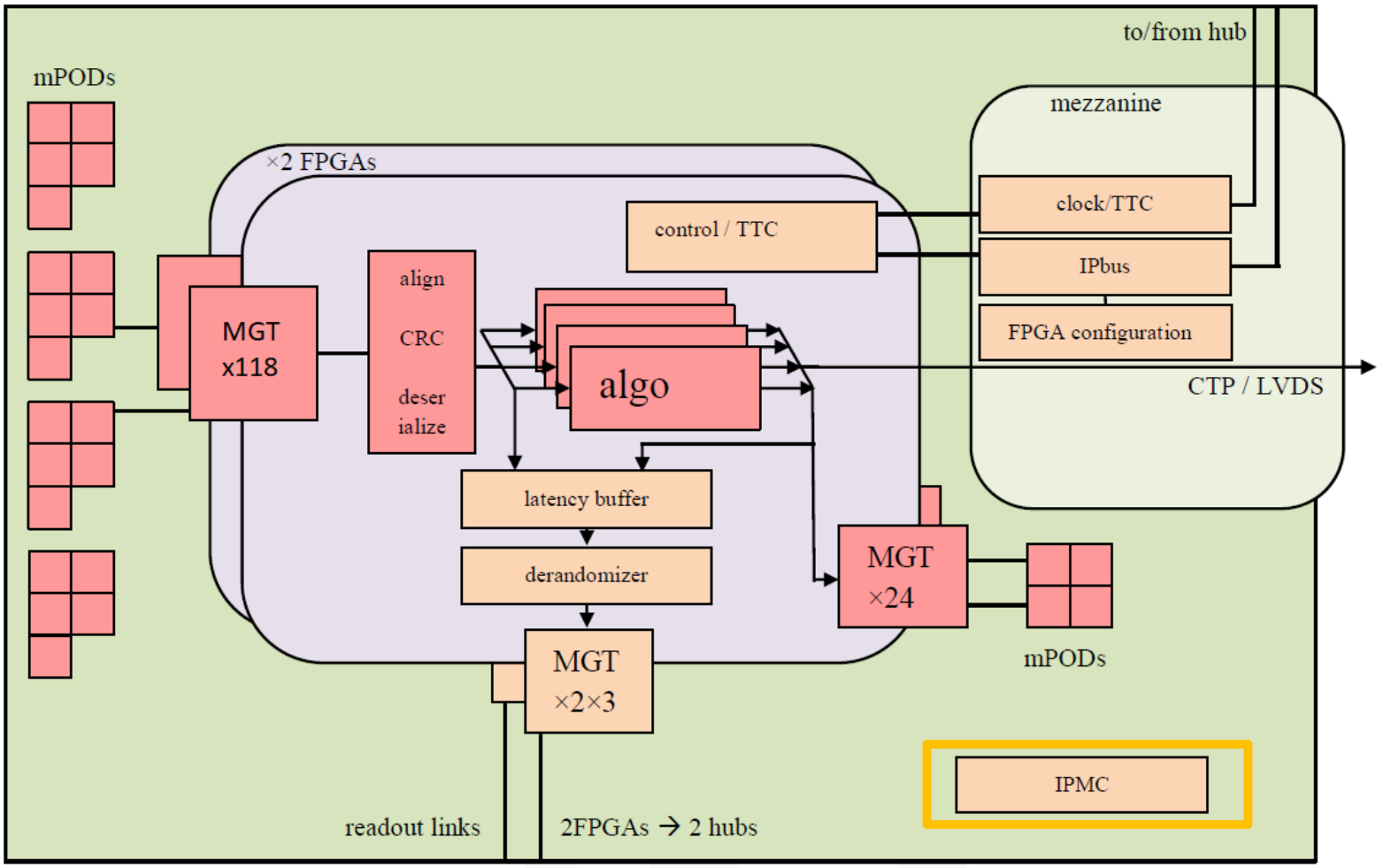
- Two processors with twelve 12-way optos each
- Extension mezzanine with added electrical out to CTP



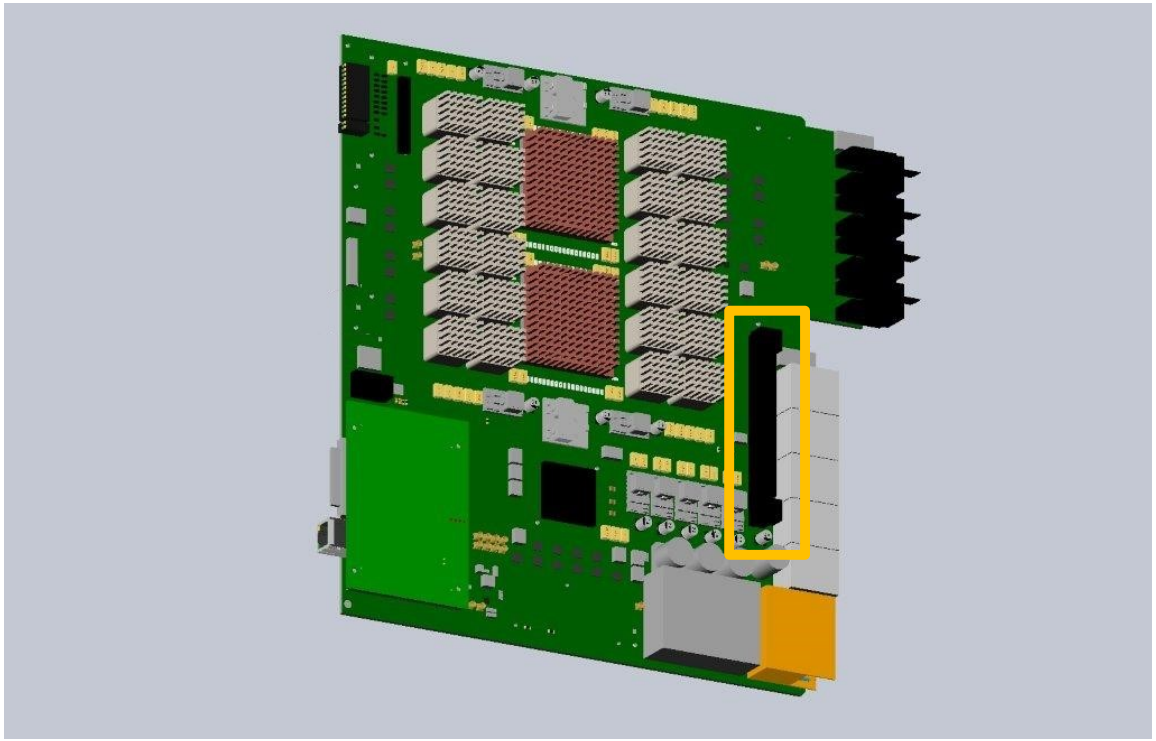
← **jFEX** 1st prototype:

- Final prototype in production
- Available MZ this month
- Both L1Topo and jFEX carry LAPP IPMC
- Probably move to a more convenient place on L1Topo

L1Topo module block diagram



L1Topo components placement



IPMC

IPMC / Environmental sensors

- IPMC design copied from current L1Topo
- IPMC not yet functional on jFEX 1st prototype.
- Under work. Adam + NN
- Coherent scheme between jFEX and new L1Topo
- All I2C sensing goes via mezzanine
- Route any vital information to the IPMC
- Probably small number of data only:
  - few voltages
  - FPGA temperatures
  - FPGA configuration status into DCS ???
- Additional expert level interface into IPbus
  - Might not be exported to DCS (tbd)

Set of required DCS data and concept of expert level access to extended data set under discussion

... Shelf level monitoring should anyway complement module level monitoring...