Just meant to start the discussion

L1Topo Phase-1

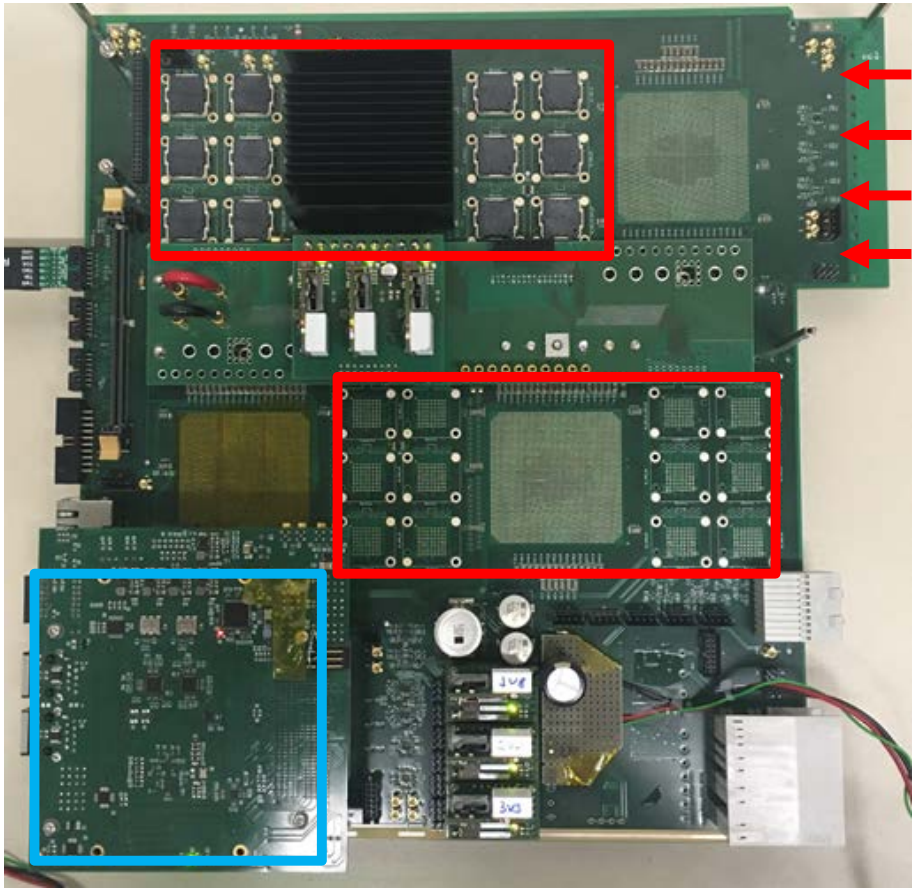
Specifications, status, review readiness

Uli / Mainz

L1Topo @ Phase-1

New **L1Topo** based on **jFEX** mainboard with

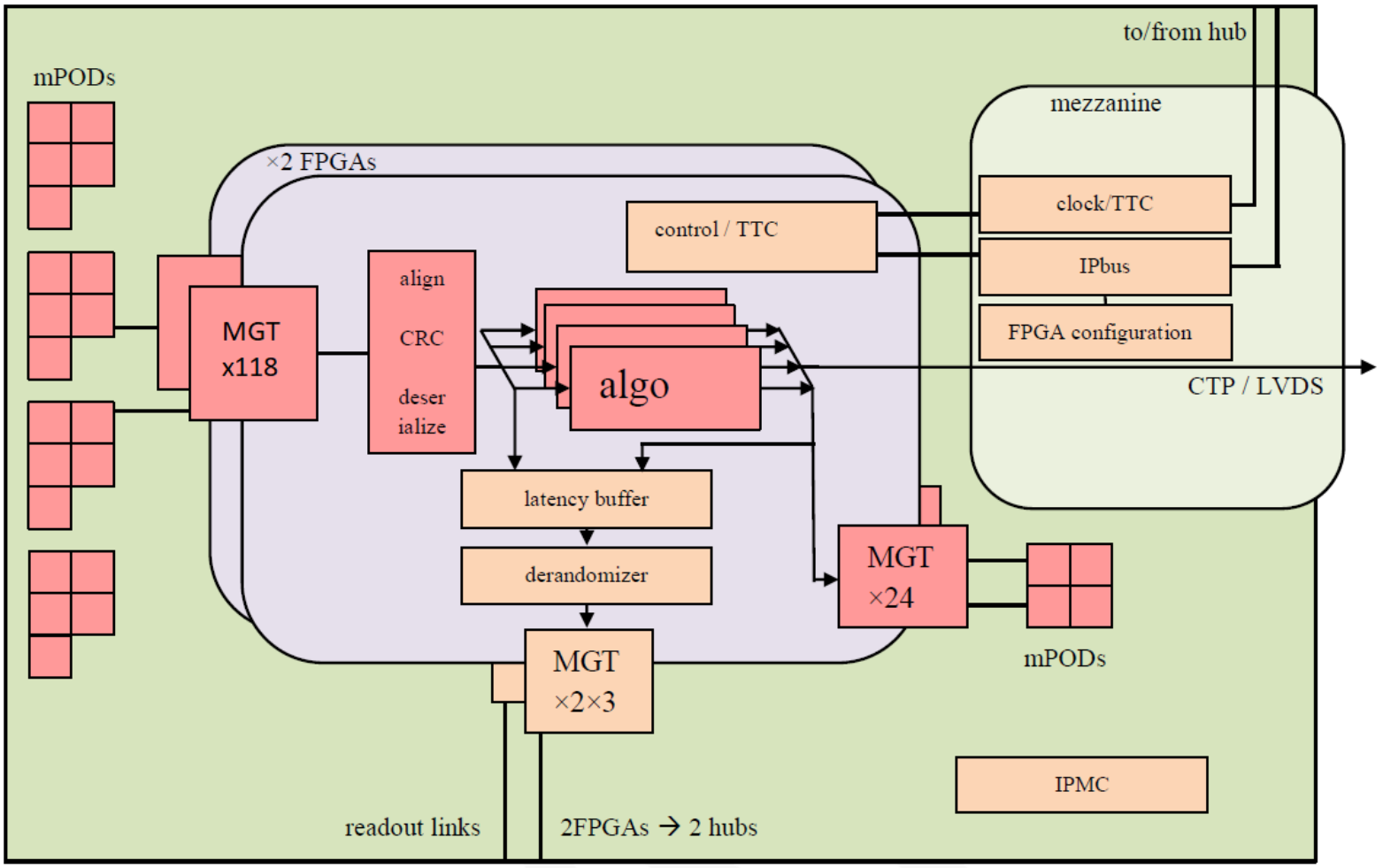
- Two processors with twelve 12-way optos each
- Extension mezzanine with added electrical out to CTP



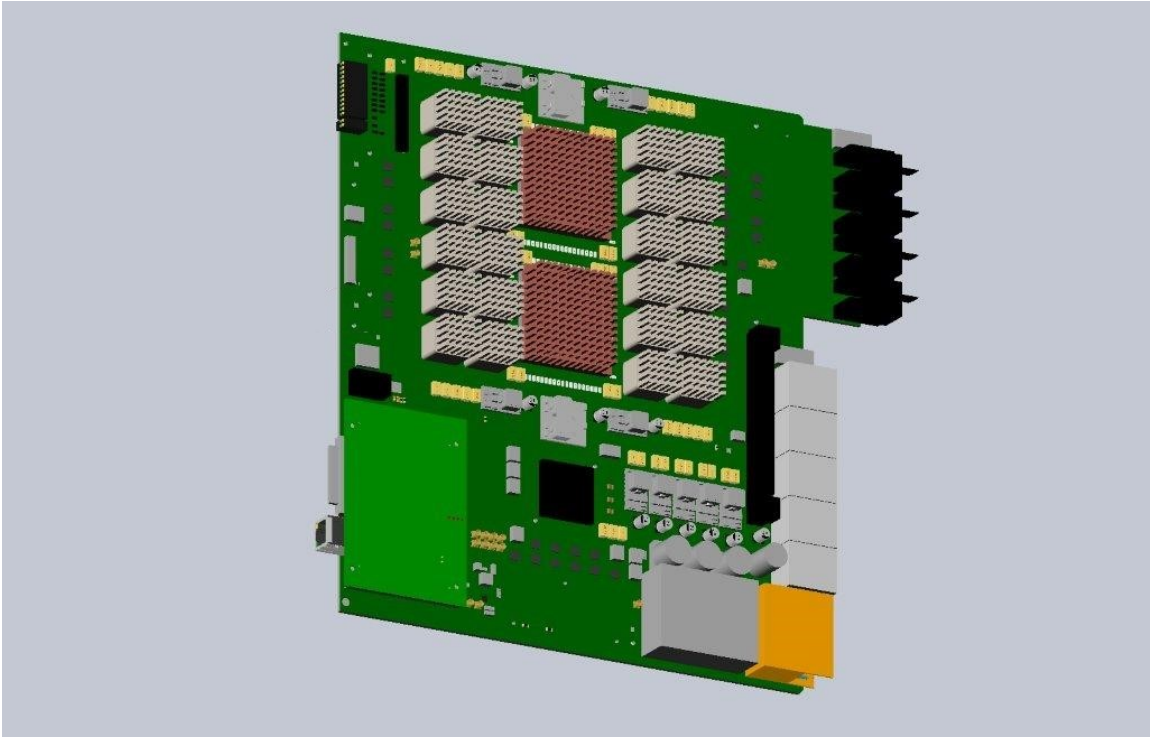
← **jFEX** prototype:

- ATCA module
- Input fibres via Zone 3
- 24 12-way opto devices
- Four processor FPGAs
- (one currently mounted)
- Control on mezzanine
- Successfully tested @CERN
- **Final prototype in production**

L1Topo module block diagram



Components placement



L1Topo @ Phase 1, some details

- ATCA modules compatible to the L1Calo Phase-1 ecosystem
- L1Calo standard ROD & clock distribution
- L1Calo standard Zone 3
- 118 input fibres per processor FPGA, 11.2/12.8 Gbps
- 24 output fibres per processor FPGA
- Electrical and optical output to CTP
- Electrical output via mezzanine / front panel
- Inter-FPGA connectivity 64 Gb/s (latency!)

- 3 L1Topo modules for Phase-1, allocated as follows
  - hit merger for L1Calo multiplicity triggers plus gFEX
  - topology : jet/tau combinations
  - topology : electron combinations
- See https://cds.cern.ch/record/2280978 (Steve H.)

Specifications

- First public draft of specs made available Aug. 04
- Review initially planned for Aug. 18
- Some comments received
- Just received a request to update the specs **before** review

Some major comments:

- Firmware documentation, including resource use
- Interface documentation
- Data formats
- Readout documentation
- Latency
- ...
- Dealing with that all before the review would move date into November

Status of h/w development

- New L1Topo is jFEX based
- jFEX schematics and layout done by Bruno B.
- Some design work on mezzanines done by Julio
- → stick to that allocation for L1Topo

- Bruno has recently restarted working on L1Topo, interleaved with jFEX work
- Expect to finish jFEX activities soon and work on L1Topo at 100%
- jFEX expected back from manufacture on Oct. 27 (so far very promising)
- Any PCB and design issues with that module would affect L1Topo as well
  - Routing layer planning (which is basically done for jFEX style sequential build)
- Block diagrams updated
- Bruno's last activity before holidays had been the MiniPOD wiring to the FPGAs (partially different from jFEX)

Firmware, effort etc.

- Christian will re-join us on Nov. 2nd : infrastructure f/w, Ipbus
- Johannes working on re-target of phase-0 L1Topo to UltraScale+ (resource use)
- Holger will be looking into online software

... and Katharina taking over Topo project management again (**now**)...