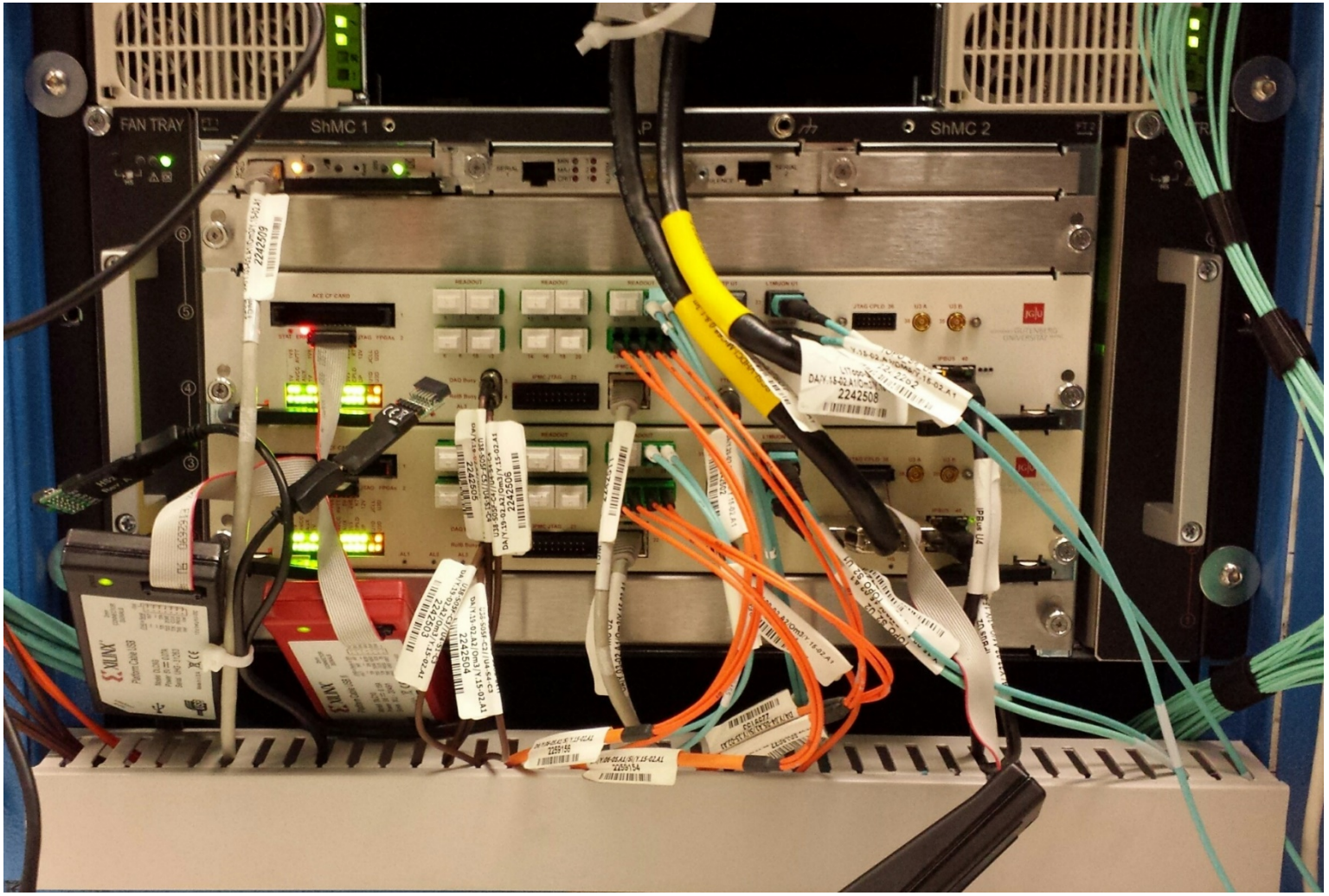
L1Topo Phase-1

Status & Plans

Uli / Mainz

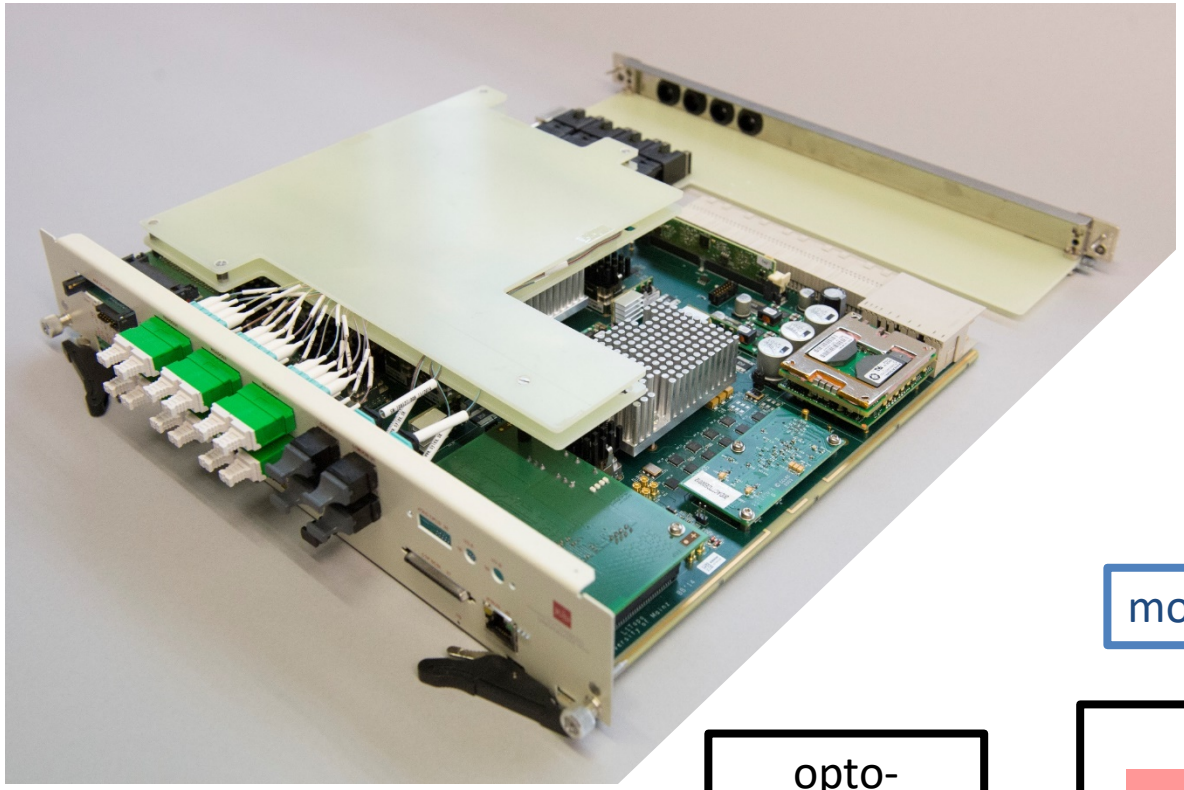
- Intro
- Interfaces / Requirements
- Status
- People
- Plans

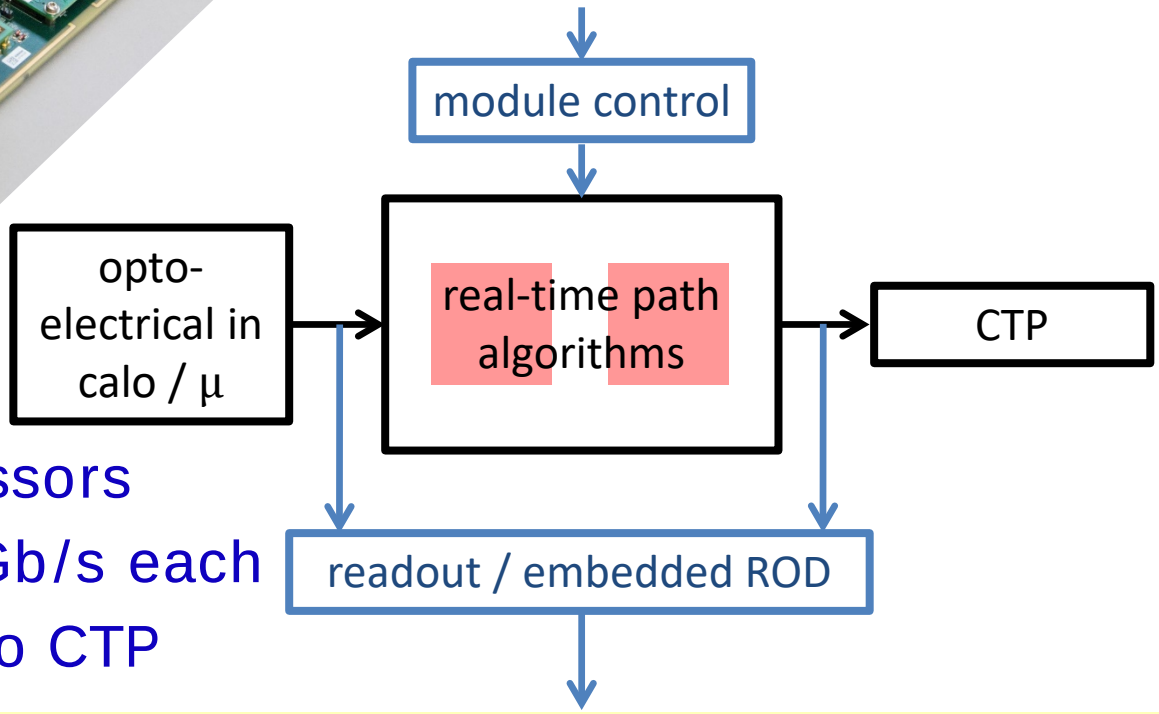
L1Topo @ Run-2



Two modules running topological algorithms, Calo & Muons
(multiplicity based Calo triggers provided by CMX)

L1Topo module @ Run-2



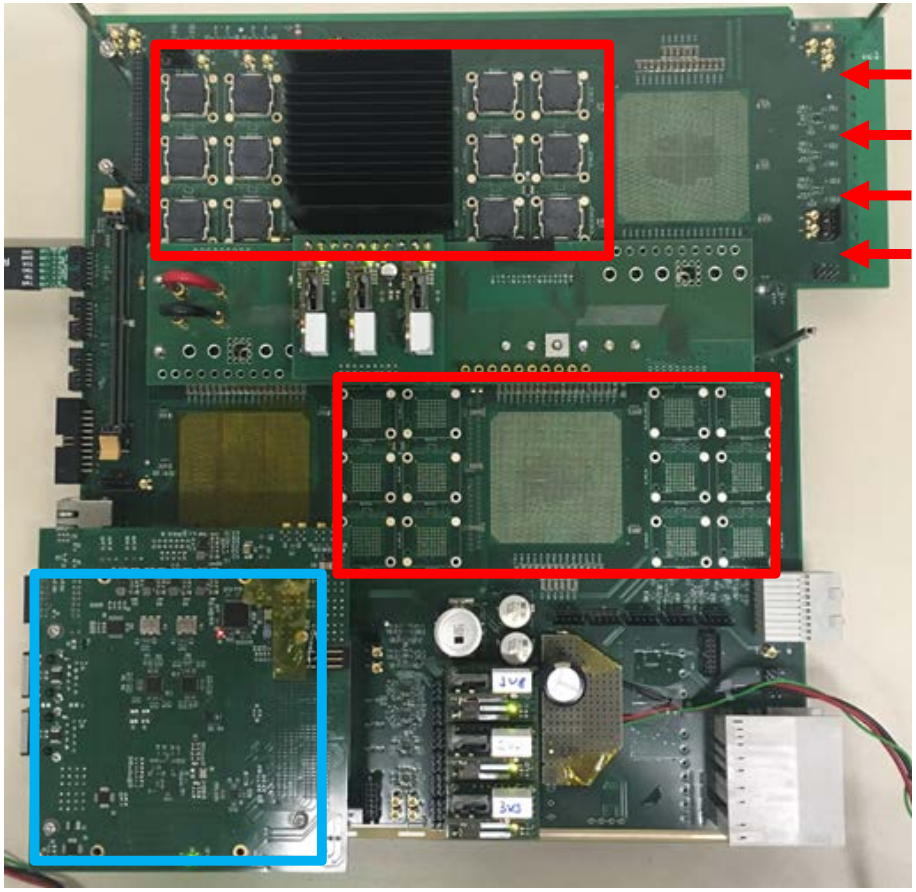


- two algorithmic processors
- 80 fibre inputs @ 6.4Gb/s each
- optical and electrical to CTP

L1Topo @ Phase-1

New **L1Topo** based on **jFEX** mainboard with

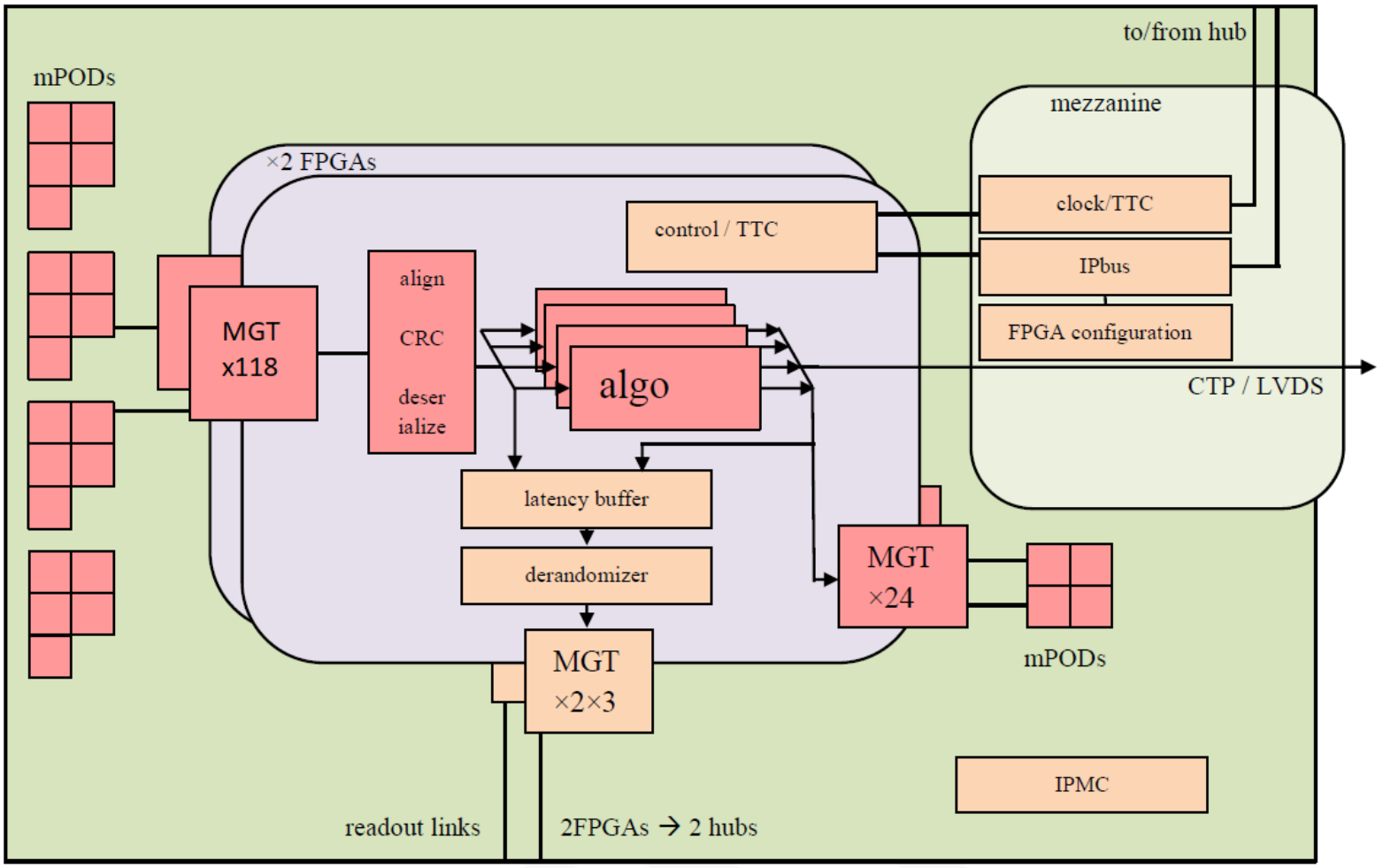
- Two processors with twelve 12-way optos each
- Extension mezzanine with added electrical out to CTP



← **jFEX** prototype:

- ATCA module
- Input fibres via Zone 3
- 24 12-way opto devices
- Four processor FPGAs
- (one currently mounted)
- Control on mezzanine
- Successfully tested @CERN
- **Final prototype in production**

L1Topo module block diagram



L1Topo @ Phase 1, some details

- ATCA modules compatible to the L1Calo Phase-1 ecosystem
- L1Calo standard ROD & clock distribution
- L1Calo standard Zone 3
- 118 input fibres per processor FPGA, 11.2/12.8 Gbps
- 24 output fibres per processor FPGA
- Electrical and optical output to CTP
- Electrical output via mezzanine / front panel
- Inter-FPGA connectivity 64 Gb/s (latency!)

That's basically the maximum possible with current technologies

- 3 L1Topo modules for Phase-1, allocated as follows (see below)
  - hit merger for L1Calo multiplicity triggers plus gFEX
  - topology : jet/tau combinations
  - topology : electron combinations

Interfaces to L1Calo and Muons

- Optical multi fibre bundles, via MPO/MTP in Zone-3, received from some re-bundling box (as current L1Topo)
- Receivers are Foxconn/Broadcom AFBR-824, 14 Gb/s
- FPGAs support >16 Gb/s
- System designed for mixed 11.2 and 12.8 Gb/s operation
  - Required by xFEX constraints
  - Muons ?
- For latency reasons 8b/10b encoding supported only
- Steve has worked out requirements regarding data volume into L1Topo from FEX/Muon sources
- Finer details of data contents / Trigger Objects (TOBs) and formats to be defined

For details on requirements see Steve's presentation:
https://indico.cern.ch/event/638444/contributions/2639285/attachments/1490897/2318031/topo170711.pdf

Status of h/w development

- New L1Topo is jFEX based
- jFEX shown to work well in current incarnation (1 FPGA)
- jFEX programme ongoing … Final prototype under way … review… preproduction… → further input into L1Topo programme

- Real work:
  - transformation jFEX → L1Topo under way
  - Have been working on routing layer planning
  - Block diagrams updated to large extent
  - Incorporate very recent updates to jFEX
  - Few things missing, need to finalize clocking

- Paper work:
  Engineering specs available soon, see below…

Who‘s who...

- Katharina – primary contact from Oct. 2017 (Uli →)
- Uli – hardware, DCS
- Johannes – firmware
- Holger – online software
- Marek – readout
- Rosa – permanently at CERN

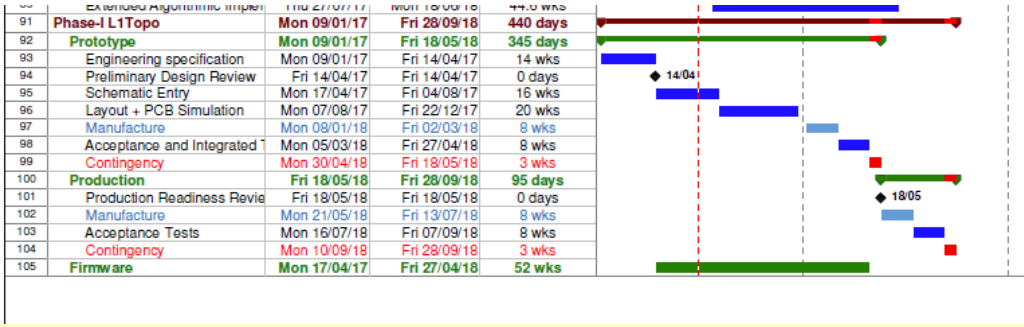
L1Topo phase-1 is a reduced jFEX hardware-wise, and an re-use/upgrade of phase-0 Topo software/firmware.

Assume synergies with jFEX project and ongoing commitment by phase-0 simulation/validation crew.

Plans (hardware)

- Hardware schedule updated
  - Specification document to be complete end July
  - PDR mid August
  - Schematics to be completed until mid October
  - Layout completed by end January
- Final hardware in hand Oct. 2018

- L1Topo and jFEX development/production cycles closely related and interleaved.



91	**Phase-I L1Topo**	**Mon 09/01/17**	**Fri 28/09/18**	**440 days**
92	**Prototype**	**Mon 09/01/17**	**Fri 18/05/18**	**345 days**
93	Engineering specification	Mon 09/01/17	Fri 14/04/17	14 wks
94	Preliminary Design Review	Fri 14/04/17	Fri 14/04/17	0 days
95	Schematic Entry	Mon 17/04/17	Fri 04/08/17	16 wks
96	Layout + PCB Simulation	Mon 07/08/17	Fri 22/12/17	20 wks
97	Manufacture	Mon 08/01/18	Fri 02/03/18	8 wks
98	Acceptance and Integrated T	Mon 05/03/18	Fri 27/04/18	8 wks
99	Contingency	Mon 30/04/18	Fri 18/05/18	3 wks
100	**Production**	**Fri 18/05/18**	**Fri 28/09/18**	**95 days**
101	Production Readiness Revie	Fri 18/05/18	Fri 18/05/18	0 days
102	Manufacture	Mon 21/05/18	Fri 13/07/18	8 wks
103	Acceptance Tests	Mon 16/07/18	Fri 07/09/18	8 wks
104	Contingency	Mon 10/09/18	Fri 28/09/18	3 wks
105	**Firmware**	**Mon 17/04/17**	**Fri 27/04/18**	**52 wks**

Further plans

Integration with external systems

- Phase-0 topo **is** integrated with external systems
- Some hardware interfaces need to be reworked
- Software/firmware interfaces to be adapted
- Assumption that for external links firmware blocks will be made available from designers of far end interface
- Readout to be adapted to ROD/hub scheme (Marek)

Simulation

- Simulation (low level, high level) exists and is being improved and maintained for current L1Topo. Will need to be continued for Phase-1 Topo. Assume that common framework will be made available for Phase-1.

Activities at Surface Test Facility

- Prototypes (very soon !) and production modules to be run at STF
- Mainz will supply
  - Modules
  - One PC specifically for Mainz controls
  - A set of USB boxes for specific controls/diagnostics (JTAG,I2C,...), probably small number of fibre bundles
  - Shelves, once production modules are there
- Once production modules and their shelves are down the pit, only spare modules and PC/USB infrastructure will remain
- Require 6-8 slots in common ATCA shelf permanently
- Expect to have access to copies of all upstream / downstream modules and expertise/effort (!!!!)
- Mainz participants in all joint STF tests: Julio, Marcel, Rosa, Uli

Schedule Test/Install/Commission

- Schedule similar to jFEX schedule, just slightly behind
- Initial (partial) system tests might be performed with Phase-0 Topo / Prototype.
- No strict need to have final L1Topo system available before complete set of upstream systems.

- People involved in CERN installations / commissioning, and long-term maintenance of Mainz built modules : Rosa, Uli

Backup slides

Latency at Phase-1

Table 13: L1Topo

	ns	BCs	Sub Total	Total	
Optical Input available from CMX, eFex, jFex & Muctpi				64,9	
L1Topo Input Deserialisers	50	2,0			
Synchronize to local clock - 320-> 40 MHz	25	1,0			
Algorithmic Processing	125	5,0			
			8,0		
Electrical Output to CTP (multiplexed) (if us	25	1,0			
Electrical Cable to CTP (if used) (2m)	10	0,4			
			1,4		
L1Topo electrical input available at CTP				74,3	L1Topo_Electrical
Output Multiplexers 40-320 MHz (if used)	25	1,0			
Output Serialisers for optics (if used)	50	2,0			
Fibres to CTP (if used) (2m)	10	0,4			
			3,4		
L1Topo Optical inputs to CTP available			11,4	76,3	L1Topo_Optical

L1Topo:

TDR figures

- Latency is tight
- Inter-FPGA fan-out is part of algo latency ! ~2BC ?
- Incoming signals on latency critical path (Muons / NSW) might bypass inter-FPGA fan-out (upstream duplication)
- Check input MGT/deserialization latency assumptions against current reality (Topo I)
- Electrical fast output path available (limited bandwidth)

Phase-2

- Seems that old plans for forward compatibility to Phase-2 have become obsolete.
- Therefore no Phase-2 slides in this presentation
- However, please note that there is plenty of optical output bandwidth available (up to 600Gb/s per L1Topo module) which is certainly not required into a Phase-1 style CTP.
- So probably well prepared for a new lease of life at Phase-2