Technical Specification

ATLAS Level-1 Calorimeter Trigger Upgrade

Topology Processor (L1Topo)

Katharina Bierwagen, Uli Schäfer

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Table of Contents

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1 Related Documents

[1.1] ATLAS TDAQ System Phase-I Upgrade Technical Design Report, CERN-LHCC-2013-018, http://cds.cern.ch/record/1602235/files/ATLAS-TDR-023.pdf

[1.2] L1Calo Phase-I Hub Specification

[1.3] L1Calo Phase-I ROD specification (*https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/Hub-ROD_spec_v0_9.pdf*)

[1.4] L1Calo Phase-I eFEX Specification (*https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/eFEX_spec_v0.2.pdf*)

[1.5] L1Calo Phase-I jFEX Specification *()*

[1.6] L1Calo Phase-I gFEX Specification *()*

[1.7] L1Calo Phase-I Optical Plant Specification

[1.8] ATCA Short Form Specification, http://www.picmg.org/pdf/picmg_3_0_shortform.pdf

[1.9] PICMG 3.0 Revision 3.0 AdvancedTCA Base Specification, *access controlled*, http://www.picmg.com/

[1.10] L1Calo High-Speed Demonstrator report (*https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/HSD_report_v1.02.pdf*)

[1.11] Development of an ATCA IPMI controller mezzanine board to be used in the ATCA developments for the ATLAS Liquid Argon upgrade, http://cds.cern.ch/record/1395495/files/ATL-LARG-PROC-2011-008.pdf

2 Conventions

The following conventions are used in this document.

A programmable parameter is defined as one that can be altered by slow control, for example, between runs, not on an event by event basis. Changing such a parameter does not require a re-configuration of any firmware.

Where multiple options are given for a link speed, for example, the readout links of the L1Topo are specified as running up to 10 Gb/s, this indicates that the link speed has not yet been fully defined. Once it is defined, that link will use a single speed. All links on the L1Topo will run at a fixed speed in the final system, but not all at the same.

In accordance with the ATCA convention, a crate of electronics here is referred to as a shelf.

3 Introduction

This document describes the specifications for the upgrade of the Level-1 topology processor module (L1Topo) of the ATLAS Level-1 Calorimeter Trigger Processor (L1Calo) [1.1] . A L1Topo processor has initially been introduced into the ATLAS trigger for Phase-0 during Run-2 to improve trigger performance by correlating trigger objects (electromagnetic clusters, jets, muons) and global quantities.

The new L1Topo will be installed in L1Calo during the long shutdown LS2, as part of the Phase-1 upgrade, and it will operate during Run 3. It is built to be forward compatible and may remain in the system after the Phase-2 upgrade in LS3, being operated in Run-4 as L1Topo or L0Topo, dependent on the eventual trigger architecture in Phase-2.

The ATLAS Phase-1 Level-1 Trigger system comprises eFEX, jFEX, and gFEX subsystems as calorimeter data sources for L1Topo. They are providing trigger object data, “TOBs”, to L1Topo via optical fibre bundles. Another source of trigger objects is the ATLAS muon trigger subsystem.

L1Topo is a set of ATCA modules, operated in a single ATCA shelf, compliant with ATLAS and L1Calo standards. Real-time data are received via optical fibres exclusively. L1Topo runs a large number of concurrent and independent algorithms on the input data, to derive a number of trigger bits, typically one result bit and one overflow bit per algorithm. The result bits are forwarded to the Central Trigger Processor, which correlates these bits with further trigger and machine data to generate Level-1 Trigger and associated data words, to be transmitted back to the detector. Outputs to CTP are available via electrical and optical data paths.

The non-real-time data paths of L1Topo are basically identical to the L1Calo modules built for Phase-1: data are sent into the readout and the 2nd level Trigger via L1Calo RODs over the backplane of the ATCA shelf. Control and global timing are accomplished via the backplane as well. To that end L1Calo communicates with two hub/ROD modules located in dedicated slots of the L1Topo shelf.

The Phase-1 Level-1 trigger system and the role of L1Topo within the Level1Calo system is described elsewhere in detail. Material on current Phase-0 L1Topo construction and performance is available as well.

4 Functionality

Figure 1 shows a block diagram of the L1Topo. The various aspects of L1Topo functionality are described in detail below. Implementation details are given in section 5.

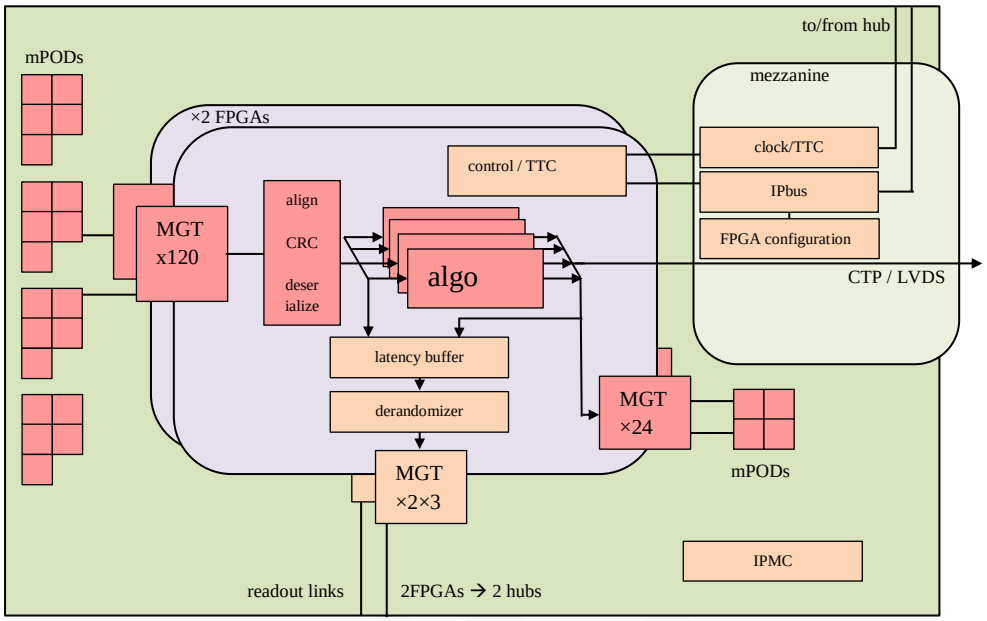

Figure 1. A block diagram of the L1Topo module.

4.1 Real-Time Data Path

ATCA Backplane zone 3 of L1Topo is used for real-time data transmission. The input data enter L1Topo optically through the backplane. The fibres are fed via four blind-mate backplane connectors that carry 48 or 72 fibres each. The optical signals are converted to electrical signals in 12-fibre receivers. For reason of design density miniPOD receivers are used. The electrical highspeed signals are routed into two FPGAs, where they are de-serialized in
MGT receivers; the parallel data are presented to the FPGA fabric. The two FPGAs operate on their input data independently and in parallel. High bandwidth, low latency parallel data paths allow for real-time communication between the two processors. The signal results are transmitted towards the CTP on both optical fibres and electrical cables. The electrical signals are routed via an extension mezzanine module.

4.1.1 Input Data

L1Topo will receive the topological output data of the sliding window processors from L1Calo and data from the L1Muon system. The data format transmitted into L1Topo comprises of TOB data (Trigger Object data) for jets, clusters and muons. The data will consist of a description of the position of an object (jet, e/m cluster, tau and muons) along with some qualifying information, like the energy sum within the object.

4.1.2 Input Data Rates

4.1.3 Algorithms

Due to the large amount of logic resources in the chosen FPGAs, a significant number of algorithms is expected to be run on the real-time data in parallel. Most of the algorithms will be identical or very similar to the once already introduced for Run-2. In addition, plenty of new and more complex algorithms can be added.

4.1.4 Data Sharing

Topology data are processed in two FPGAs. There is no data duplication implemented at PCB level. The two processors can communicate via a parallel bus to get access to data that cannot be received directly via the multi-gigabit links. Though according to the device data sheets higher data rates should be possible, a maximum bit rate of xxx Gb/s per differential pair is anticipated for the inter-FPGA link. That will limit parallel connectivity to xxx Gb/s of aggregate bandwidth. This would correspond to xxx bits per BX (xxx bits) which allow for sharing more than 250 generic trigger objects (TOBs) according to the current L1Topo. This is more than the outputs of all of the sort trees combined.

4.1.5 Output

The real-time output data of the L1Topo to the CTP consist of individual bits indicating whether a specific algorithm passed or not plus an overflow bit. The resulting trigger data are expected to exhibit a rather small volume. They will be transmitted to CTP optically or electrically. A single fibreoptical ribbon connection per module that carry 48 fibres, running through the front panel of the module is provided for this purpose. A mezzanine board will be required to interface L1Topo to the CTPCORE module electrically via 32 LVDS signals at low latency.

4.2 Error Handling

Errors will be monitored and the error counter will be incremented for any clock cycle where there is at least one error in any input channel. Afterwards the error flags will be set back to 0. Detailed information of the specific error will be stored in expert registers.

4.3 Latency

A breakdown of the estimated latency of the real-time path of the L1Topo is given in the ATLAS TDAQ System Phase-1 Upgrade Technical Design Report [1.1] .

4.4 Readout Data Path

A detailed description of the readout data path is given in xxx.

4.5 TTC and Clock

TTC signals are received in the L1Topo shelf in the Hub-ROD module. There, the clock is recovered and commands are decoded, before being re-encoded using a local protocol (to be defined). This use of a local protocol allows the TTC interface of the shelf to be upgraded without any modification of the L1Topo modules.

The L1Topo module receives the clock and TTC commands from the Hub-ROD via the ATCA backplane. It receives the clock on one signal pair and the commands on a second (see section 5.10 for details).

4.6 Slow Control and Configuration

An IPBus interface is provided for high-level, functional control of the L1Topo. This allows, for example, algorithmic parameters to be set, modes of operation to be controlled and spy memories to be read.

IPBus is a protocol that runs over Ethernet to provide register-level access to hardware. Here, it is run over a 1000BASE-T Ethernet port, which occupies one channel of the ATCA Base Interface. On the L1Topo there is a local IPBus interface in every FPGA, plus the IPMC. These interfaces contain those registers that pertain to that device. The Merger FPGA implements the interface between the L1Topo and the shelf backplane, routing IPBus packets to and from the other devices as required. The Merger FPGA also contains those registers which control or describe the state of the module as a whole. For those devices such as MiniPODs, which have an I^2C control interface, an IPBus-I2C bridge is provided.

4.7 Commissioning and Diagnostic Facilities

To aid in module and system commissioning, and help diagnose errors, the L1Topo can be placed in Playback Mode (via an IPBus command). In this mode, real-time input data to the L1Topo are ignored and, instead, data are supplied from internal scrolling memories. These data are fed into the real-time path at the input to the feature-extracting logic, where they replace the input data from the calorimeters.

Optionally, the real-time output of the L1Topo can also be supplied by a scrolling memory. It should be noted that, in this mode, the L1Topo will process data from one set of memories, but the real-time output will be supplied by a second set of memories. Depending on the content of these memories, this may result in a discrepancy between the real-time and readout data transmitted from the L1Topo.

In Playback Mode the use of the input scrolling memories is mandatory, the use of the output scrolling memories is optional, and it is not possible to enable Playback Mode for some channels but not others. Playback Mode is selected, and the scrolling memories loaded, via the slow control interface. The scrolling memories are 256 words in depth.

In addition to the above facility, numerous flags describing the status of the L1Topo can be read via the slow control interface (see section **Fehler! Verweisquelle konnte nicht gefunden werden.**). Access points are also provided for signal monitoring, boundary scanning and the use of proprietary FPGA tools such as ChipScope and IBERT.

4.8 Environmental Monitoring

The L1Topo monitors the voltage and current of every power rail on the board. It also monitors the temperatures of all the FPGAs, of the MiniPOD receivers and transmitters, and of other areas of dense logic. Where possible, this is done using sensors embedded in the relevant devices themselves. Where this is not possible, discrete sensors are used.

The voltage and temperature data are collected by the L1Topo IPMC, via an I^2C bus. From there, they are transmitted via IPBus to the ATLAS DCS system. The L1Topo hardware also allows these data to be transmitted to the DCS via IPMB and the ATCA Shelf Controller, but it is not foreseen that ATLAS will support this route.

If any board temperature exceeds a programmable threshold set for that device, IPMC powers down the board payload (that is, everything not on the management power supply). The thresholds at which this function is activated should be set above the levels at which the DCS will power down the module. Thus, this mechanism should activate only if the DCS fails. This might happen, for example, if there is a sudden, rapid rise in temperature to which the DCS cannot respond in time.

4.9 ATCA form factor

The L1Topo is an ATCA module, conforming to the PICMG® 3.0 Revision 3.0 specifications.

5 Implementation

The description of the implementation is based on L1Topo modules in the central region. Details of the implementation differ on modules covering the outer regions, due to changes in the input data granularity and the η coverage.

5.1 Modular Design

5.2 Input Data Reception

The L1Topo receives data from the calorimeters via optical fibres. Each fibre carries data from an area of 0.4×0.4 (η, ϕ). In order to cover an area as described in section 5.1, a single L1Topo module must receive data on up to 192 fibres. Two modules require up to 16 additional links, carrying the data from the Tile-HEC overlap, making a total of 208.

The input fibres to the L1Topo are organised into 18 ribbons of 12 fibres each. They are routed to the L1Topo via the rear of the ATCA shelf, where a rear transition module provides mechanical support. Optical connections between the fibres and the L1Topo are made by up to four 72-way Multi-fibre Push-On/Pull-Off (MPO) connectors, mounted in Zone 3 of the ATCA backplane. These connectors allow the L1Topo to be inserted into, and extracted from, the shelf without the need to handle individual ribbon connections.

On the L1Topo side of the MPO connectors, 18 optical ribbons (each comprising 12 fibres) carry the signals to 18 Avago MiniPOD receivers. These perform optical to electric conversion. They are mounted on board, around the Processor FPGAs, to minimise the length of the multi-Gb/s PCB tracks required to transmit their output. If the positioning on the PCB does not allow using MiniPODs, the smaller MicroPODs are used instead.

Each of the received signals is transmitted to two of the four Processor FPGAs. The Processor FPGA, which has a core region that covers the region in ϕ from which the data on a fibre is originated, receives the incoming signal. The data is retransmitted to one of the neighbouring Processor FPGAs via "PMA loopback". Once the signal has been received by the FPGA and equalisation has been performed, but before the signal has been decoded, it is sent from the high-speed receiver to the paired high-speed transmitter. There is a latency penalty of >25 ns and some degradation of signal quality associated with this method. The L1Topo must therefore handle upwards of 416 multi-Gb/s signals.

5.3 Processor FPGA

There are four Processor FPGAs on the L1Topo. The functionality they implement can be grouped into real-time, readout and slow-control functions. All Processor FPGAs on a L1Topo module have the same functionality. The differences between the Processor FPGAs on different modules are caused by the varying core areas covered by a certain module and are implemented via different firmwares.

Every Processor FPGA performs the following real-time functions.

- It receives, from MiniPOD optical receivers, up to 104 inputs of serial data at 12.8 Gb/s and additional data for the extended environment from neighbouring FPGAs on 1Gb/s differential links. These carry data from the calorimeters, from an environment of 2.8×3.6 (3.9×3.6 in forward region).
- It applies the feature-identification algorithms described in section 4.1.2 to the calorimeter data, to identify and characterise jet and τ objects and calculate global values.
- For each jet and τ object found, it produces a TOB, as described in section **Fehler! Verweisquelle konnte nicht gefunden werden.**.
- It prioritises the TOBs, and if the number it has found exceeds the number that can be transmitted to the Merger FPGA in one BC, the excess TOBs are supressed.
- It transmits its TOB results to the Merger FPGA via 48 differential signal pairs at a bandwidth of 1Gb/s per pair.

Each Processor FPGA can process a core area of calorimeter data of 0.8×1.6 (2.9×1.6 in the forward regions). The differences between the modules depending on their covered η range are implemented via firmware. The hardware is the same for all modules.

On the readout path (described in section 4.1), each Processor FPGA performs the following functions.

- The Processor FPGA records the input data and the TOBs generated on the real-time path in scrolling memories, for a programmable duration of up to 3 μs.

- On receipt of an L1A, it writes data from the scrolling memories to the FIFOs, for a programmable time frame. This is only done for those data enabled for readout by the control parameters.
- The Processor FPGA transmits data from the readout FIFOs to the Merger FPGA, via a 12.8GB/s MGT link.

For slow control and monitoring, each Processor FPGA contains a local IPBus interface, which provides access to registers and RAM space within the FPGAs.

The Processor FPGA is a Xilinx XCVU190. The dominant factor in the choice of device is the available number of multi-Gb/s receivers, low latency parallel links and logic resources.

Of the 120 high speed links available in the XCVU190, depending on the covered η range, 80 to 104 are used. The spare resources can be used for slow control functions, to further reduce the required number of parallel links.

Regarding general-purpose I/O, of the 448 pins available 408 pins can be used for differential links. A maximum of 96 are required to transport real-time output data, 84 are required to transmit/receive pile-up sums, 56 are required to transmit/receive additional data from the extended environment, 50 are planned for slow control functions. The remaining 122 pins are left for spare resources. In case of a latency penalty at high bit rates, these spare resources can be used to decrease the transmission speed on latency critical connections. Up to 96 additional pins are required if different data are to be sent to the two FPGAs on an L1Topo module.

5.4 Clocking

There are two types of clock sources on L1Topo: on-board crystal clocks and the LHC TTC clock, received from the ATCA backplane. These clock sources are fed via the clocking circuitry to five FPGAs. The 40.08MHz TTC clock has too much jitter to drive multi-Gb/s links directly. A PLL chip is therefore used to clean up the jitter on this clock. From the input of 40.08 MHz the PLL chip can generate clocks of frequency $n \times 40.08$ MHz within a certain range. This flexibility allows the multi-Gb/s links on the L1Topo to be driven at a large range of different rates. The TI CDCE62005 has been tested and verified on the High-Speed Demonstrator [1.10] and thus is considered an option for the L1Topo. Another option is the Si5326 which is currently used on the L1Topo.

To facilitate standalone tests of the high-speed serial links on the L1Topo, an on-board crystal clock of 40.08MHz is also provided.

The reference clocks for the MGTs on both the Processor FPGAs and the Merger FPGA are driven by PLL chips. The readout links will probably run at a slower speed than the real-time links, as they are copper links over an ATCA backplane. Therefore, the readout links and real-time links are driven with separate PLL chips.

A 125MHz crystal clock is provided for the Merger FPGA for its Gigabit Ethernet interface to the shelf IPBus network. On the L1Topo, the protocol between the IPBus master (in the Merger FPGA) and the IPBus slaves (in the other FPGAs) runs using this clock. Hence, the L1Topo module control function over IPBus is independent from the TTC clock domain.

The 40.08MHz clock and its multiples (e.g. 160.32MHz or 320.64MHz) from a PLL chip are also connected to the global clock inputs of all the Processor FPGAs and the Merger FPGA.

5.5 High-Speed signals on the PCB

The L1Topo is a very high-speed and very high-density ATCA module, which has about 450 optical fibre links running at a speed of 12.8Gb/s, and many copper links running up to 12.8Gbps over the backplane. In addition, the tight ATLAS L1Calo latency margin requires hundreds of parallel links running at up to 1Gb/s between FPGAs for results merging and data sharing on the L1Topo.

Signal integrity is a big challenge for the L1Topo design. The designing will be accompanied by detailed PCB simulations.

5.6 FPGA configuration

The L1Topo houses five big FPGAs: four Processor FPGAs and the Merger FPGA. The configuration of these FPGAs is done using a small device (microcontroller or another FPGA). This device contains an integral flash memory from which it loads its configuration data on power up. (These data are downloaded to this memory during commissioning of the L1Topo, via the JTAG Boundary Scan port.) In case an additional FPGA is used as the Configurator, the firmware loaded into the Configurator is Xilinx System ACE *SD Controller* IP. Once configured it becomes a System ACE controller, responsible for the configuration process of the other FPGAs on the L1Topo. It initiates this process as soon as it, itself, is configured.

The configuration data for the five FPGAs are stored on the L1Topo in a micro SD flash card. They are stored as collections of firmware, where one collection comprises one firmware load for each FPGA on the L1Topo, excluding the Configurator. Up to eight firmware collections can be stored on the L1Topo and handled by the Configurator. The collections are enumerated and by default collection zero is loaded into the FPGAs. This choice can be over-written by IPBus. Currently, only two firmware collections are foreseen for the L1Topo: the normal, running-mode firmware and a diagnostic collection. Extra capacity for a further six collections is spare. The configuration data stored in the micro flash SD card can be updated via IPBus.

Re-configuration of the FPGAs can be initiated via IPBus and via the low-level management IPMI bus. The Configurator must be re-configured separately from the other FPGAs, which must be re-configured as a group. As the IPBus interface is implemented in the Merger FPGA, and the firmware of the Merger FPGA can be updated over IPBus, it is possible, by uploading bad firmware, to place the L1Topo in a non-working state from which it cannot be recovered via IPBus. For this reason a firmware collection that is known to work should always be kept in the micro flash SD. This ensures it is always possible to restore the L1Topo to a working state via the IPMI bus.

5.7 The IPM Controller

For the purposes of monitoring and controlling the power, cooling and interconnections of a module, the ATCA specification defines a low-level hardware management service based on the Intelligent Platform Management Interface standard (IPMI). The Intelligent Platform Management (IPM) Controller is that portion of a module (in this case, the L1Topo) that provides the local interface to the shelf manager via the IPMI bus. It is responsible for the following functions:

- interfacing to the shelf manager via dual, redundant Intelligent Platform Management Buses (IPMBs), it receives messages on all enabled IPMBs;
- negotiating the L1Topo power budget with the shelf manager and powering the Payload hardware only once this is completed (see section 5.8);
- managing the operational state of the L1Topo, handling activations and deactivations, hot-swap events and failure modes;
- implementing electronic keying, enabling only those backplane interconnects that are compatible with other modules in shelf, as directed by the shelf manager;
- providing to the Shelf Manager hardware information, such as the module serial number and the capabilities of each port on backplane;
- collecting, via an I^2C bus, data on voltages and temperatures from sensors on the L1Topo, and sending these data, via IPBus, to the Merger FPGA;
- driving the ATCA-defined LEDs.

The L1Topo uses the IPMC mezzanine produced by LAPP as the IPM Controller [1.11] . The form factor of this mezzanine is DDR3 VLP Mini-DIMM.

5.8 Power Management

With regard to power, the hardware on the L1Topo is split into two domains: Management hardware and Payload hardware. The Management hardware comprises the IPM Controller plus the DC-DC converters and the non-volatile storage that this requires. By default, on power up, only the Management hardware of the L1Topo is powered (drawing no more than 10 W), until the IPM Controller has negotiated power-up rights for the Payload hardware with the shelf manager. This is in accordance with the ATCA specification. However, via a hardware switch it is also possible to place the L1Topo in a mode where the Payload logic is powered without waiting for any negotiation with the shelf controller. This feature, which is in violation of the ATCA specification, is provided for diagnostic and commissioning purposes.

On power-up of the Payload hardware, the sequence and timing with which the multiple power rails are turned on can be controlled by the IPM Controller. Alternatively, by setting hardware switches, these rails can be brought up in a default sequence defined by resistor-capacitor networks on the module.

Excluding the optional exception noted above, the L1Topo conforms to the full ATCA PICMG® specification (issue 3.0, revision 3.0), with regard to power and power management. This includes implementing hot swap functionality, although this is not expected to be used in the trigger system.

Power is supplied to the L1Topo on dual, redundant -48V DC feeds. Two Emerson ATC250 (or similar) convertors accept these feeds and provide a power supply of 3.3 V to the Management hardware, and a supply of 12V to the Payload hardware. This 12V supply is stepped down further, by multiple switch-mode regulators, to supply the multiplicity of voltages required by the payload hardware.

For the power supplies to the FPGA multi-Gigabit transceivers, the PCB design guidelines and noise requirements specified in the UltraScale Series FPGAs GTH Transceiver User Guide (UG576) and GTY Transceiver User Guide (UG578) will be observed.

5.9 Front-panel Inputs and Outputs

The following signals are, or can be, input to the L1Topo via the front panel.

- Auxiliary clock. This input allows the L1Topo to be driven by an external 40 MHz clock, in the absence of a suitable clock on the backplane. The optimum physical form factor for the signal is to be identified.

The following bi-directional control interfaces are available on the front panel. See section 5.12 for the use of these interfaces.

- JTAG Boundary Scan. The optimum physical form factor for this interface is to be identified.
- 1G Ethernet socket.

5.10 Rear-panel Inputs and Outputs

5.10.1 ATCA Zone 1

This interface is configured according to the ATCA standard. The connections include

- dual, redundant -48V power supplies,
- hardware address,
- IPMB ports A and B (to the Hub module),
- shelf ground,
- logic ground.

Figure 2 shows the backplane connections between the L1Topo and the Hub module, which are located in Zones 1 and 2 of the ATCA backplane. See the ATCA specification for further details.

5.10.2 ATCA Zone 2

5.10.2.1 Base Interface

The Base Interface comprises eight differential pairs. Four of these are connected to hub slot one and are used for module control, the other four are connected to hub slot two and are used to carry DCS traffic. Both of these functions are implemented using IPBus, running over 1G Ethernet links.

5.10.2.2 Fabric Interface

The Fabric Interface comprises 16 differential signal pairs, eight of which are connected to hub slot one, and eight of which are connected to hub slot two. Those signal pairs connected to hub slot one are used as follows:

- One signal pair is used to receive the TTC clock.
- One signal pair is used to receive decoded TTC commands, plus near real-time signals such as ROD busy. The protocol is to be defined. The link speed does not exceed 10 Gb/s.
- Six signal pairs are used to transmit readout data. The link speed does not exceed 10 Gb/s. Two out of these six signal pairs are used as receivers in standard ATCA backplanes. They are inverted to increase the possible readout bandwidth.

Those signal pairs connected to hub slot two are reserved for the same functions as above. Potentially, this allows redundant connections to be made to this hub slot. However, the firmware necessary to drive and receive data to and from the Fabric Interface of hub slot two is undeveloped.

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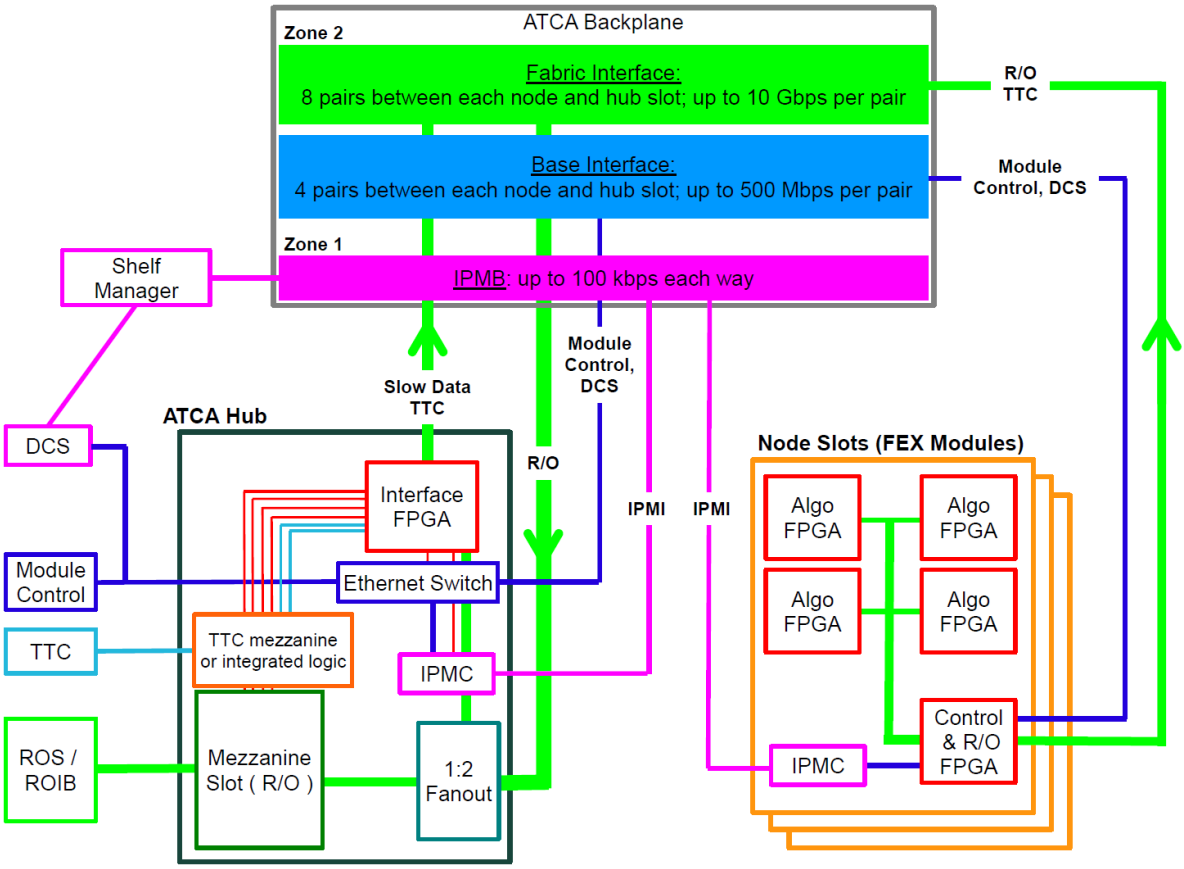

Figure 2. The ATCA backplane connections between the L1Topo and the Hub module.

5.10.3 ATCA Zone 3

ATCA zone houses four 72-way optical MPO connectors. Three of these house a total of up to 208 fibres, carrying data from the calorimeters to the L1Topo (see section 5.1). At the rear of the MPO connectors, optical fibres carry data from the calorimeters to the L1Topo via the L1Calo Optical Plant. These fibres are supported in the L1Topo shelf by a (passive, mechanical) rear transition module (RTM). On the L1Topo side of the connectors, fibre ribbons carry the calorimeter data to MiniPOD receivers, mounted in board. The optical connections are made on the insertion of the L1Topo into the shelf, and broken on its extraction. The fourth MPO connector houses fibres, carrying TOB data from the Merger FPGA to the L1Topo modules.

5.11 LEDs

All LEDs defined in the ATCA specifications are located on the L1Topo front panel. In addition, further status LEDs are provided on either the front panel or the top side. These indicate functions like power, Done signals, L1A receipt und further LEDs for diagnostic purposes for all FPGAs.

5.12 Instrument Access Points

5.12.1 Set-Up and Control Points

The following interfaces are provided for the set-up, control and monitoring of the L1Topo. They are intended for commissioning and diagnostic use only. During normal operation it should not be necessary to access the L1Topo via these interfaces.

- The JTAG Boundary Scan port: via this port a boundary scan test can be conducted, all FPGAs on the L1Topo can be configured, the configuration memory of the Configurator can be loaded and the FPGA diagnostic/evaluation tool ChipScope can be run, including for IBERT tests. This port is on the front panel.
- The 1G Ethernet port: this port provides an auxiliary control interface to the L1Topo, over which IPBus can be run, should there be a problem with, or in the absence of, an IPBus connection over the shelf backplane. It is on the front panel and connected to the Merger FPGA.
- The RS232 port: this port provides a control interface of last resort, available if all others fail. It is mounted on the top side of the module and connects to the Merger FPGA. Firmware to implement this interface will only be developed if needed.

5.12.2 Signal Test Points

Due to the sensitive nature of multi-Gb/s signals, no test points are provided on PCB tracks intended to carry multi-Gb/s data. If such signals need to be examined, this must be done via firmware. Test points are placed on a selection of those data and control tracks that are not operating at multi-Gb/s.

For each FPGA, spare, general-purpose IO pins are routed to headers. Furthermore, spare multi-Gb/s transmitters and receivers are routed to SMA sockets. With appropriate firmware these connections allow internal signals, or copies of data received, to be fed to an oscilloscope, for example, or driven from external hardware.

The exact number of test connections, and those signals on which a test point can be placed most usefully, are to be determined during schematic entry.

5.12.3 Ground Points

At least six ground points are provided, in exposed areas on the top side of the module, to allow oscilloscope probes to be grounded.

5.13 Floor plan

Figure 3 shows a preliminary floor plan of the L1Topo module. This will be used as a guide for the layout process; the exact location of components may change as the physical constraints on the layout are better understood.

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The routing of over 400 signals at multi-Gb/s presents a significant challenge for the design of the L1Topo PCB. In order to minimise track lengths and routing complexity for these signals, the Avago MiniPOD receivers are placed around the Processor FPGAs. However, this creates an additional constraint on the layout: the need to accommodate routing paths for the fibre-optic ribbons carrying the data to these receivers. To connect the MPO connectors to the receivers the ribbons need to twist, curve and bypass large heat sinks on the FPGAs. It can be seen in Figure 3 that large components have been excluded from some areas of the floor plan, to allow space for the routing of the fibre-optic ribbons.

In addition to those components shown in Figure 3, glue logic is placed on the underside of the module.

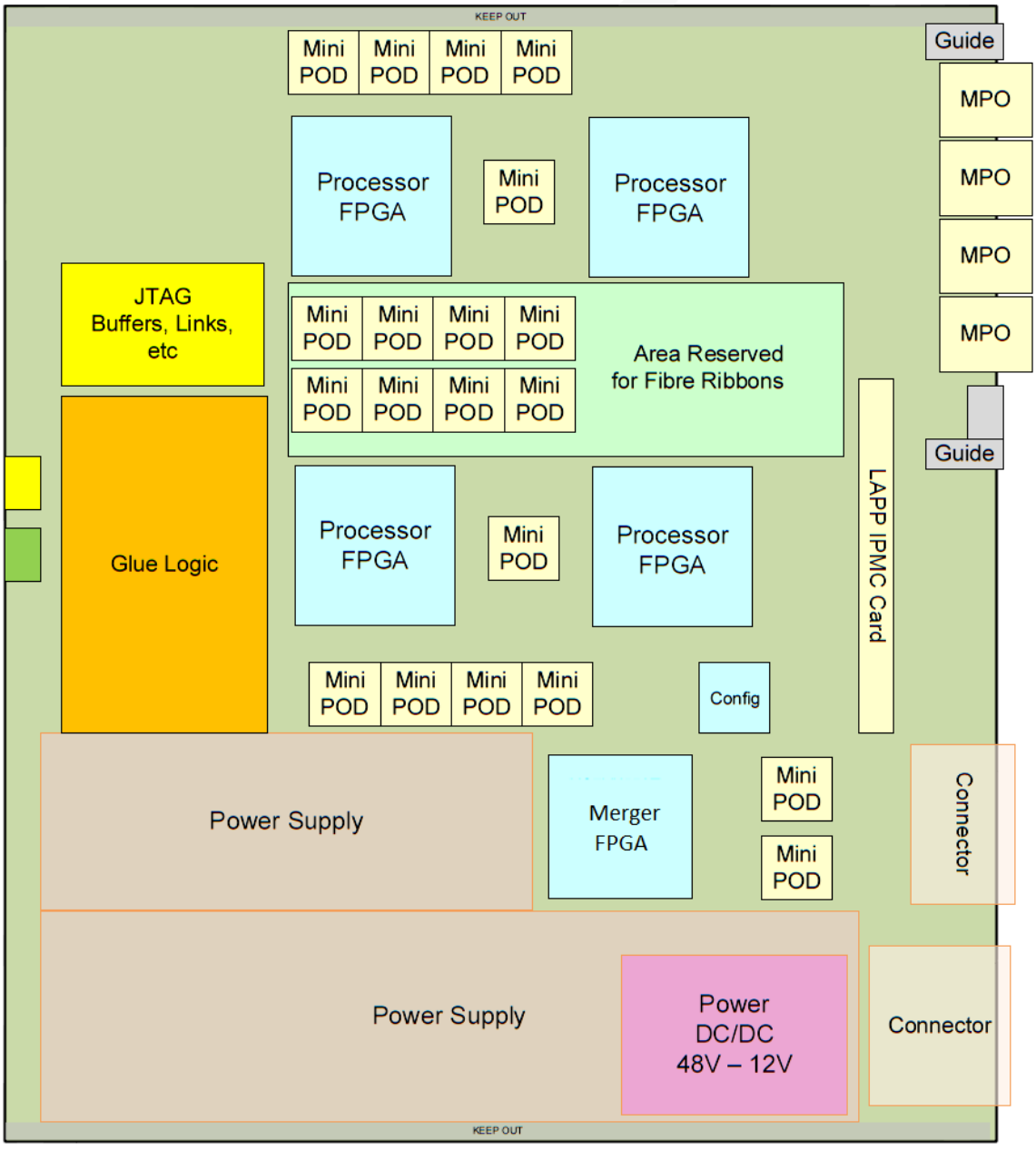

Figure 3. A floor plan of the L1Topo, showing a preliminary placement guide.

6 Front-Panel Layout

Figure 4. Preliminary front panel layout (not to scale).

Figure 4 shows a preliminary template for the front panel layout of the L1Topo. Shown are the JTAG port for boundary scanning and FPGA access, an auxiliary Ethernet control port, status LEDs and the ATCA extraction/insertion handles. These components are not drawn to scale.

7 Glossary

ATCA	Advanced Telecommunications Computing Architecture (industry standard).
BC	Bunch Crossing: the period of bunch crossings in the LHC and of the clock provided to ATLAS by the TTC, 24.95 ns.
BCMUX	Bunch-crossing multiplexing: used at the input to the CPM, JEM (from Phase 1) and eFEX, this is a method of time-multiplexing calorimeter data, doubling the number of trigger towers per serial link.
CMX	Common Merger Extended Module.
CP	Cluster Processor: the L1Calo subsystem comprising the CPMs.
CPM	Cluster Processor Module.
DAQ	Data Acquisition.
DCS	Detector Control System: the ATLAS system that monitors and controls physical parameters of the sub-systems of the experiment, such as gas pressure, flow-rate, high voltage settings, low-voltage power supplies, temperatures, leakage currents, etc.
ECAL	The electromagnetic calorimeters of ATLAS, considered as a single system.
eFEX	Electromagnetic Feature Extractor.
FEX	Feature Extractor, referring to either an eFEX or L1Topo module or subsystem.
FIFO	A first-in, first-out memory buffer.
FPGA	Field-Programmable Gate Array.
HCAL	The hadronic calorimeters of ATLAS, considered as a single system.
IPBus	An IP-based protocol implementing register-level access over Ethernet for module control and monitoring.

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IPMB	Intelligent Platform Management Bus: a standard protocol used in ATCA shelves to implement the lowest-level hardware management bus.
IPM Controller	Intelligent Platform Management Controller: in ATCA systems, that portion of a module (or other intelligent component of the system) that interfaces to the IPMB.
IPMI	Intelligent Platform Management Interface: a specification and mechanism for providing inventory management, monitoring, logging, and control for elements of a computer system. A component of, but not exclusive to, the ATCA standard.
JEM	Jet/Energy Module.
JEP	Jet/Energy Processor: the L1Calo subsystem comprising the JEMs.
L1Topo	Jet Feature Extractor.
JTAG	A technique, defined by IEEE 1149.1, for transferring data to/from a device using a serial line that connects all relevant registers sequentially. JTAG stands for Joint Technology Assessment Group.
L0A	In Run 4, the Level-0 trigger accept signal.
L0Calo	In Run 4, the ATLAS Level-0 Calorimeter Trigger.
L1A	The Level-1 trigger accept signal.
L1Calo	The ATLAS Level-1 Calorimeter Trigger.
LHC	Large Hadron Collider.
MGT	As defined by Xilinx, this acronym stands for Multi-Gigabit Transceiver. However, it should be noted that it denotes a multi-gigabit transmitter–receiver pair.
MiniPOD	An embedded, 12-channel optical transmitter or receiver.
MicroPOD	An embedded, 12-channel optical transmitter or receiver, smaller compared to the MiniPOD.
MPO	Multi-fibre Push-On/Pull-Off: a connector for mating two optical fibres.
PMA	Physical Media Attachment: a sub-layer of the physical layer of a network protocol.
ROD	Readout Driver.
RoI	Region of Interest: a geographical region of the experiment, limited in η and ϕ, identified by the Level-1 trigger (during Run 3) as containing candidates for Level-2 trigger objects requiring further information. In Run 4, RoIs are used in the same between the Level-0 and Level-1 triggers.
Shelf	A crate of ATCA modules.
SMA	Sub-Miniature version A: a small, coaxial RF connector.
Supercell	LAr calorimeter region formed by combining E_T from a number of cells adjacent in η and ϕ.
TOB	Trigger Object.

TTC	The LHC Timing, Trigger and Control system.
XTOB	Extended Trigger Object. A data packet passed to the readout path, contained more information than can be accommodated on the real-time path.

8 Document History

Version	Comments
0.0	Internal circulation

9 Interfaces

9.1 Internal Interfaces

9.2 External Interfaces

10 Data formats

The formats of the data received and generated by the L1Topo have yet to be finalised. Those defined here are working assumptions only.

10.1 Input Data

The L1Topo modules receive data from the calorimeters on optical fibres. For the region $|\eta| < 2.4$

Data from the calorimeters are transmitted to the L1Topo as continuous, serial streams. To convert these streams into parallel data, the L1Topo logic must be aligned with the word boundaries in the serial data. The scheme for achieving this is yet to be defined, but there are a number of possible mechanisms. For example, boundary markers can be transmitted during gaps in the LHC bunch structure. These markers are substituted for zero data and are interpreted as such by the L1Topo trigger-processing logic. Periodic insertion of such markers allows links to recover from temporary losses of synchronisation automatically.

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10.2 Real-Time Output Data

The Real-time output of the L1Topo comprises TOBs, each of which contains information about a jet or τ candidate, such as its location and the deposited energy. Figure 5, Figure 8 and Figure 9 show the draft format of the jet TOB, fat jet TOB and τ TOB respectively. Besides these candidates the global values, E_T and E_T^{miss}, are transferred to L1TOPO. They are sent separately as E_T, E_T^X and E_T^Y as 13-bit energy values.

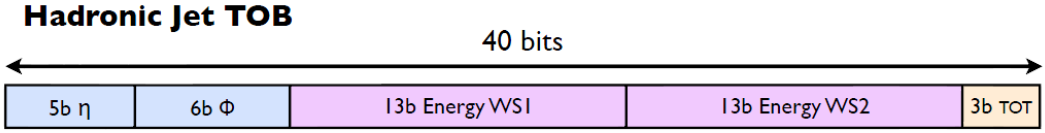
Due to multiple jet finding algorithms, the jet TOBs include two energies. The results from two algorithms, which are based on the same seeding procedure, can be compressed into one TOB. The sizes of the remaining TOBs are adjusted to match the jet TOBs.

The TOBs are transmitted to L1Topo on optical fibres. The line rate and protocol used for this transmission is the same as that used to transmit data from the calorimeters to the L1Topo. The baseline specification is thus as follows.

- The data are transferred across the optical link at a line rate 12.8 Gb/s.
- 8b/10b encoding is used to maintain the DC balance of the link and ensure there are sufficient transitions in the data to allow the clock recovery.
- Word-alignment markers (8b/10b control words) are inserted periodically, as substitutes for zero data.

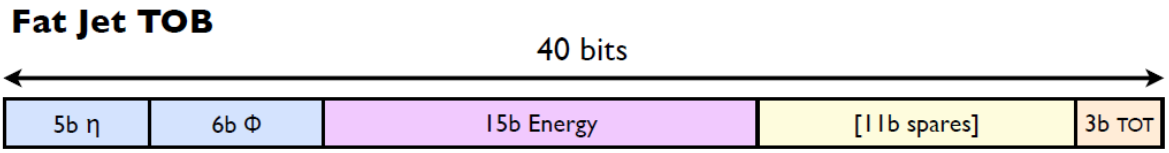
For TOBs of 40 bits, four links at the given specifications allow a maximum of 24 TOBs and the global values to be transmitted to L1Topo per bunch crossing.

Should the specification of the L1Topo inputs change, the specification of the real-time outputs will be updated to match. (Using a common line rate and encoding scheme enables the output data to be looped back to the inputs for diagnostic purposes.)



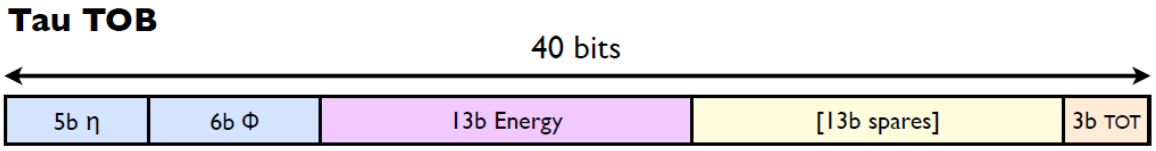
TOB contents	No. Bits	Comments
η	5	Local η coordinate, within core area of jFEX
Φ	6	Global Φ coordinate
Energy WS1	13	Energy computed for window size 1
Energy WS2	13	Energy computed for window size 2
Trigger Object Type (TOT)	3	Trigger object : Had. Jet, Fat Jet, tau
TOTAL	**40**	

Figure 5. Draft jet TOB Format.



TOB contents	No. Bits	Comments
η	5	Local η coordinate, within core area of jFEX
Φ	6	Global Φ coordinate
Energy	15	Energy
[spares]	11	Spare bits TBD final use
Trigger Object Type (TOT)	3	Trigger object : Had. Jet, Fat Jet, tau
TOTAL	**40**	

Figure 6. Draft fat jet TOB Format.



TOB contents	No. Bits	Comments
η	5	Local η coordinate, within core area of jFEX
Φ	6	Global Φ coordinate
Energy	13	Energy
[spares]	13	Spare bits TBD final use
Trigger Object Type (TOT)	3	Trigger object : Had. Jet, Fat Jet, tau
TOTAL	**40**	

Figure 7. Draft τ TOB format.

10.3 Readout Data

On receipt of an L1A, the L1Topo transmits to the ROD a packet of data of the format shown in Figure 1. This packet contains up to three types of data: TOBs, XTOBs and input data (see below). The TOBs are exact copies of those output from the L1Topo on the real-time path.

The input data are copies of the calorimeter data as received in the Processor FPGAs. The XTOBs are words that contain more information about trigger candidates than can be transmitted on the real-time data path. If the readout of XTOBs is enabled, any TOB in the readout data will have a corresponding XTOB. The readout data may also contain XTOBs for which there is no corresponding TOB. Such XTOBs describe trigger candidates for which TOBs have not been transmitted to L1Topo because of the input bandwidth limit of that module. The exact format of the XTOBs is yet to be determined. Preliminary assumptions introduce a width of up to 64 bits.

The data in the readout packet are from a programmable window of bunch crossings. The size of this window is the same for all types of data and is limited by the available memory in the Processor FPGAs. The size can be set via control parameters.

Within the packet, the data are organised first according to type, and then according to bunch crossing. Headers mark the boundaries between data types and bunch crossings. Not every type of data is necessarily present in a packet. If a data type is absent, then the headers for that data are also absent. In the extreme, the packet may contain no data, in which case just the packet header and footer are transmitted.

The L1Topo readout packets are transmitted to the ROD via six links at up to 10 Gb/s per link, using a link-layer protocol that is to be defined.

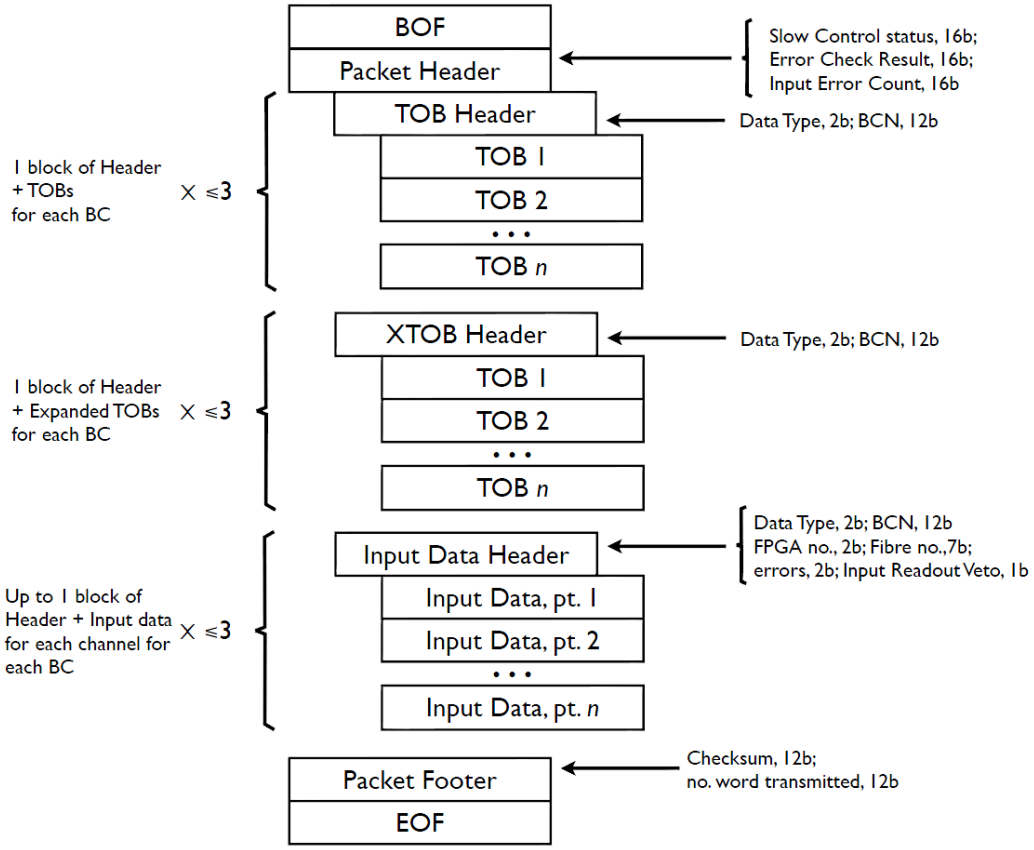


Figure 1. A provisional format for a readout data packet.