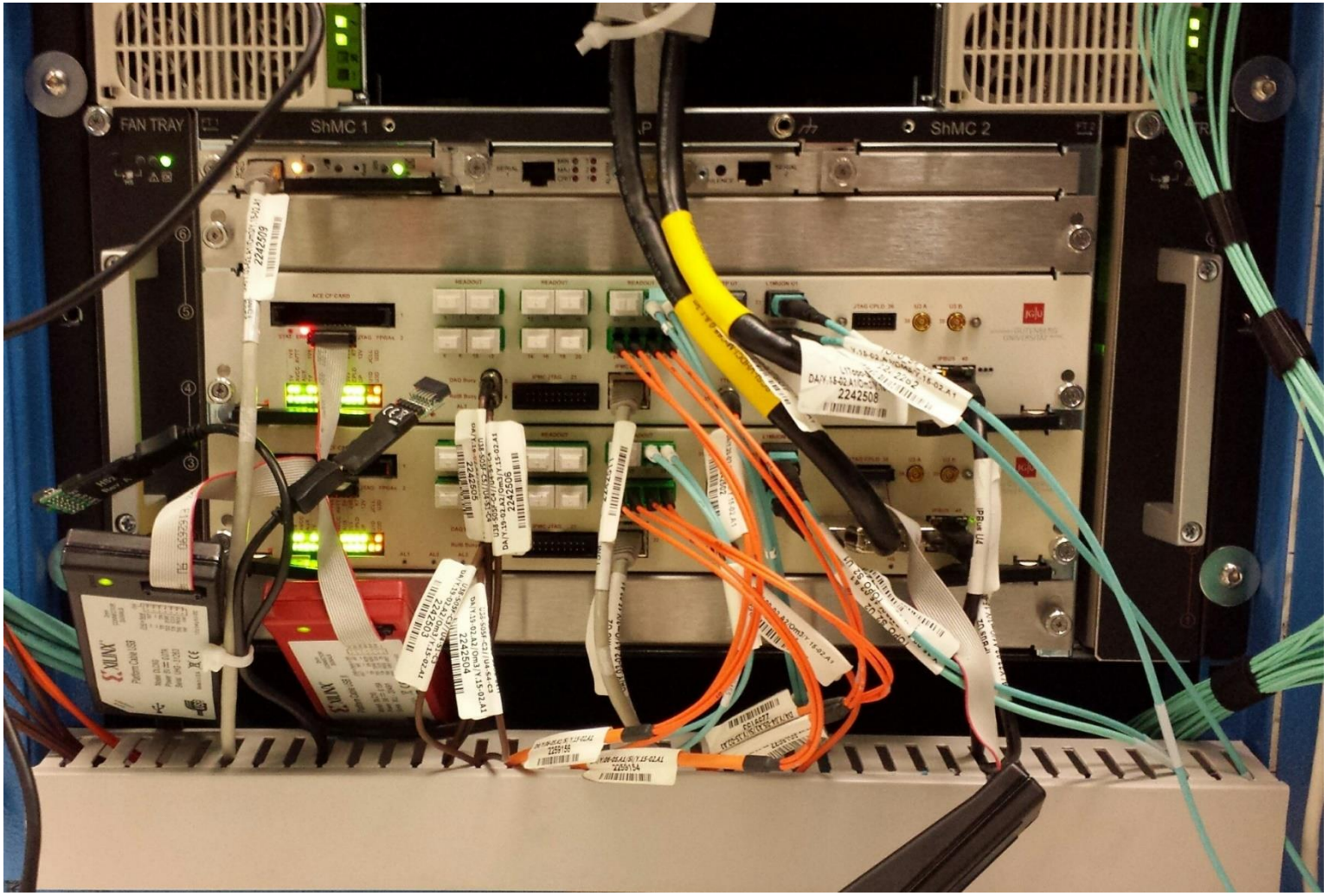
L1Topo Phase-1

Status & Interfaces

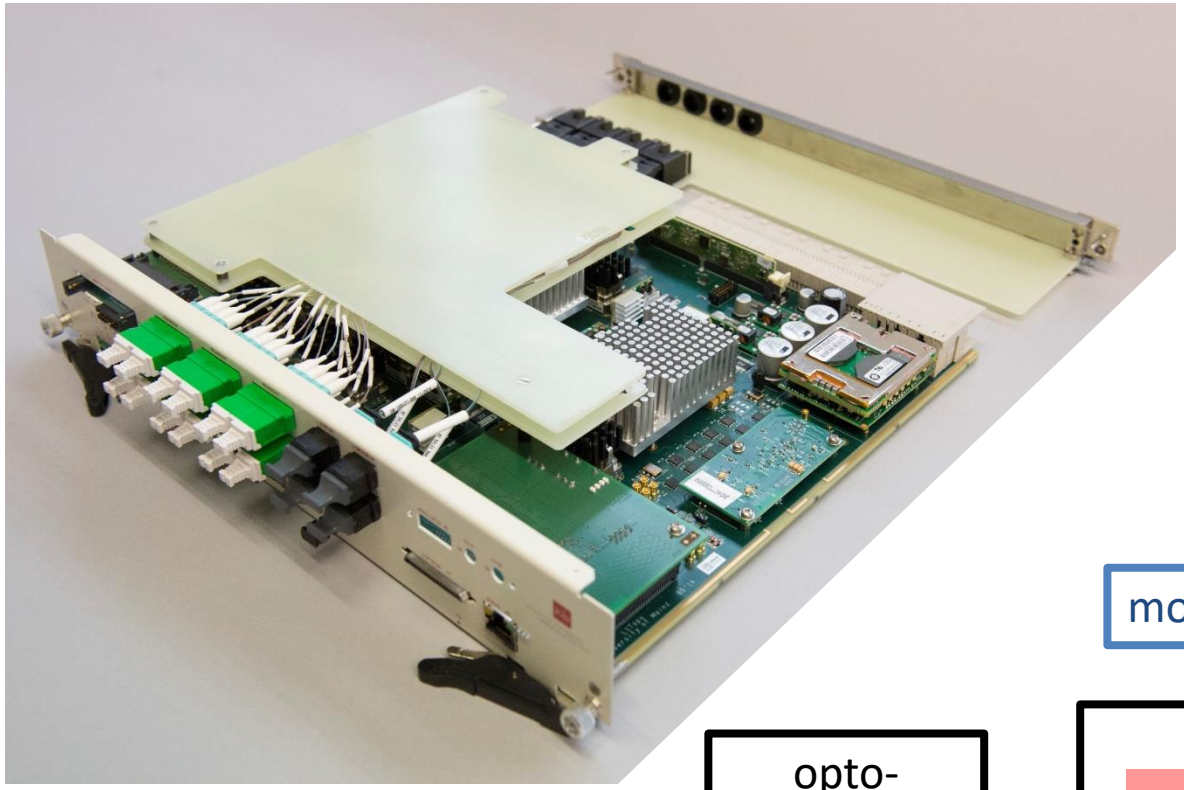
Uli / Mainz

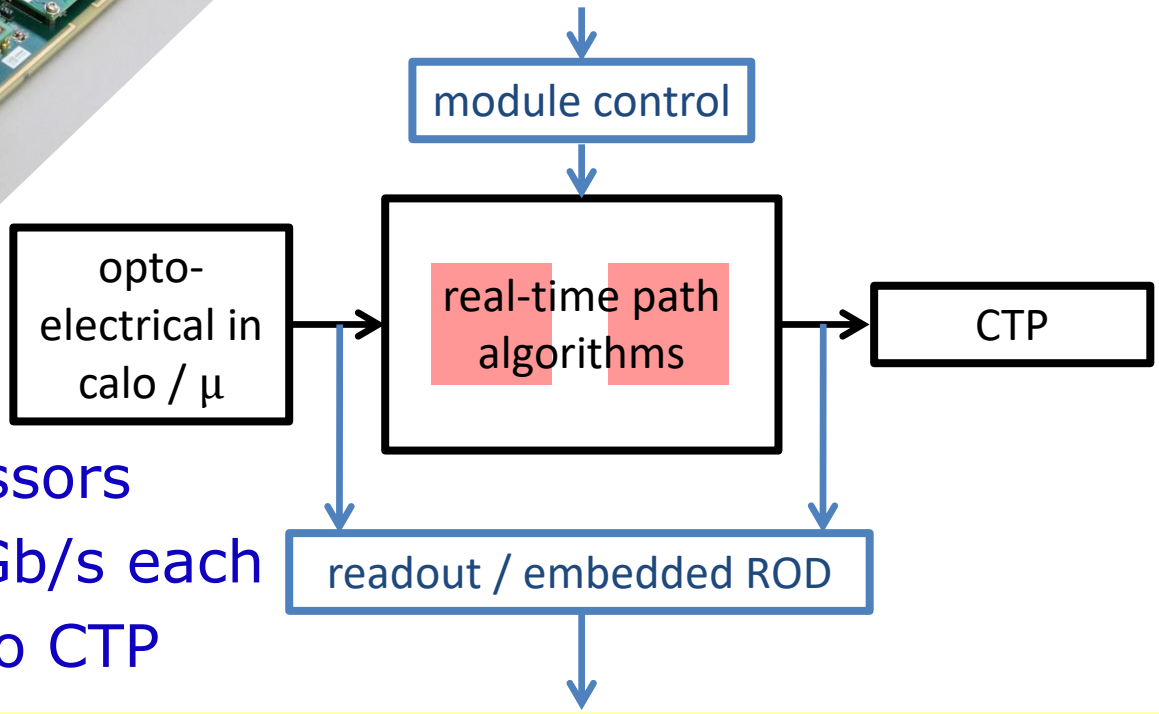
L1Topo @ Run-2



Two modules running topological algorithms, Calo & Muons
(multiplicity based Calo triggers provided by CMX)

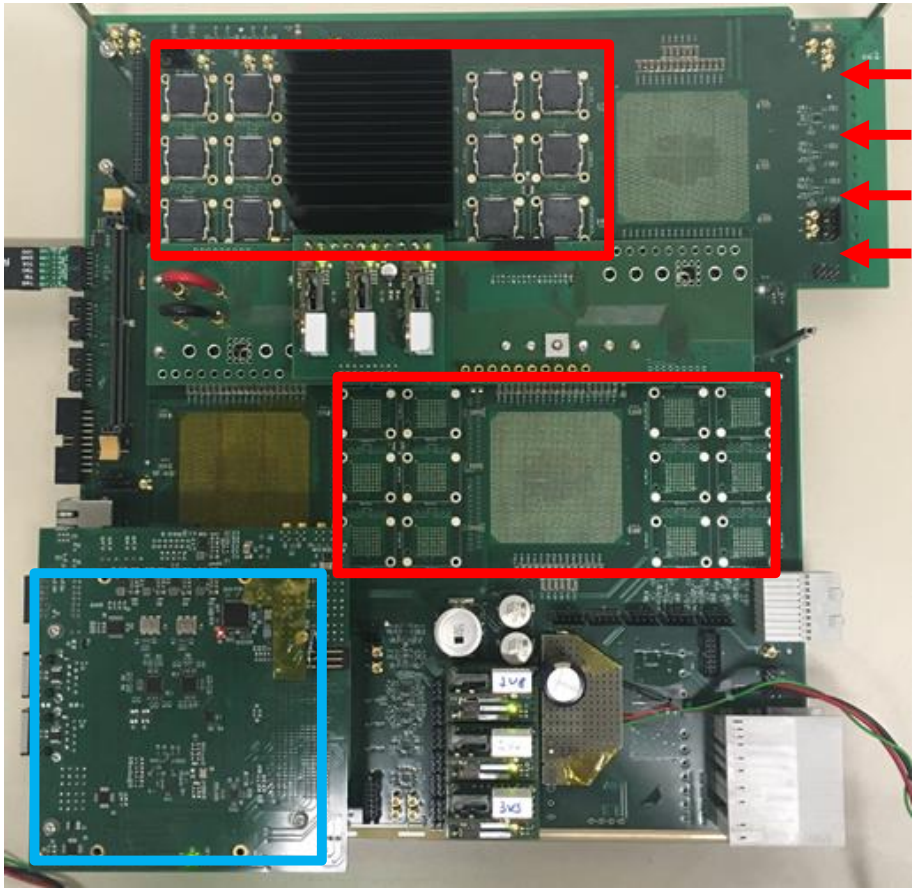
L1Topo module @ Run-2





- two algorithmic processors
- 80 fibre inputs @ 6.4Gb/s each
- optical and electrical to CTP

L1Topo @ Phase-1



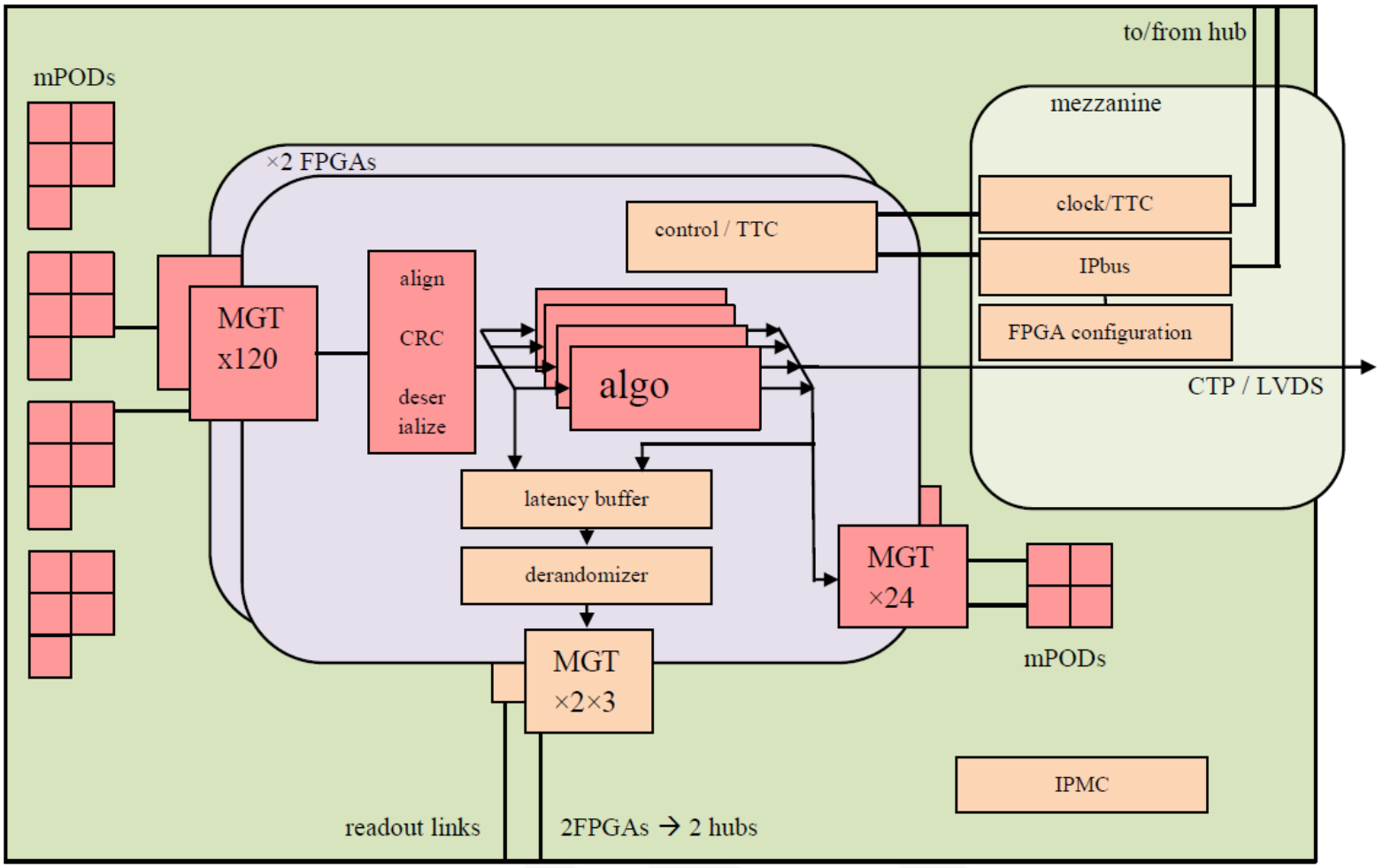
← jFEX prototype

- ATCA module
- Input fibres via Zone 3 ←
- 24 12-way opto devices
- Four processors
- (one currently mounted)
- Control on mezzanine
- Successfully tested @CERN

New L1Topo based on jFEX mainboard with

- Two processors with twelve 12-way optos each
- Extension mezzanine with added electrical out to CTP

L1Topo module block diagram



L1Topo @ Phase 1, some details

- ATCA modules compatible to the L1Calo Phase-1 ecosystem
- L1Calo standard ROD & clock distribution
- L1Calo standard Zone 3
- 120 input fibres per FPGA processor
- 24 output fibres per FPGA processor
- Designed for mixed 11.2/12.8Gbps environment
- Electrical and optical output to CTP
- Electrical output via mezzanine / front panel
- Some, but limited inter-FPGA connectivity (latency!)

That's basically the maximum possible with current technology

- 3 L1Topo modules were initially planned for Phase-1
  - 2 × topology
  - 1 × hit merger for L1Calo multiplicity triggers

Further: see slides on L1Topo specification task force

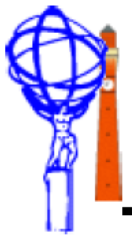
Interfaces to L1Calo and Muons

- Optical multi fibre bundles, via MPO/MTP in Zone-3
- Receivers are Foxconn/Broadcom AFBR-824, 14 Gb/s
- FPGAs support up to 16 Gb/s
- System designed for mixed 11.2 and 12.8 Gb/s operation
  - Required by xFEX constraints
  - Muons ?
- For latency reasons 8b/10b encoding supported only
- L1Topo specifications task force (Steve H.) has set requirements regarding data volume into L1Topo
- Fine details of data contents (and formats) to be defined

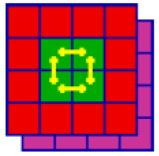
Report on specifications taskforce activities and results at recent L1Calo meeting, and draft requirements document:

https://indico.cern.ch/event/598198/contributions/2483149/attachments/1419514/2174908/topo170228.pdf
https://indico.cern.ch/event/598198/contributions/2483149/attachments/1419514/2174678/toporequirements.pdf

Data contents… example…



eFEX outputs



- 24 modules, 2 x 16 fibre outputs
  - Various options for partitioning of outputs possible
  - My current preferred option:
    - 1 x high priority/threshold EM TOBs
    - 1 x low+high priority/threshold EM TOBs
    - 1 x high priority/threshold TAU TOBs
    - 1 x low+high priority/threshold TAU TOBs
- Each link contains up to 7 objects
  - eFEX coverage about 2x current CPM
    - CPM saturates at 5 TOBs (only occasionally an issue for EM3)
    - eFEX saturation at 7+7 TOBs should be easily sufficient
      - For Phase-1 anyway, may need re-think for Phase-2
- With 4 different link outputs, 8 copies are possible
  - More than enough to feed 2 FPGAs in 4 Topos

Data into L1Topo, summary

TOB type	Fibres	Copies	Name
Muon TOBs	8	6	MU
EM TOBs (high priority)	24	8	EM1
EM TOBs (low priority)	24	8	EM2
Tau TOBs (high priority)	24	8	TAU1
Tau TOBs (low priority)	24	8	TAU2
Jet TOBs (first fibre)	28	4	JET1
Jet TOBs (second fibre)	28	4	JET2
jFEX Missing/Total Energy	14	4	XE
gFEX jet TOBs and global quantities	8	6	GFEX

Maximum number of data (in terms of fibres) supplied by respective processor systems. Ideally one copy of data supplies one L1Topo processor FPGA exclusively.

Here direct outputs from upstreams processors are assumed. No optical splitting.

Allocation of L1Topo input bandwidth

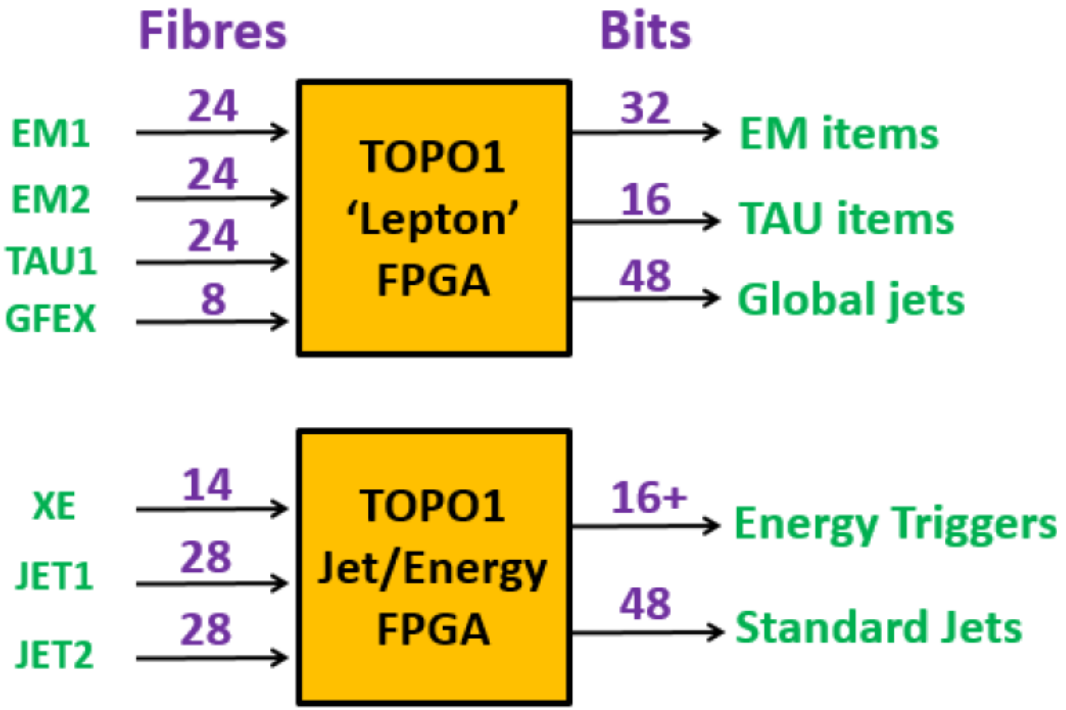
- Assume 3 L1Topo modules
- Two processor FPGAs each

- Multiplicity based triggers
- Simple, few-TOB-type algorithms
- Heavy stuff, require it all…

How to get data into L1Topo (1)

‘Simple’ TOPO1 Module

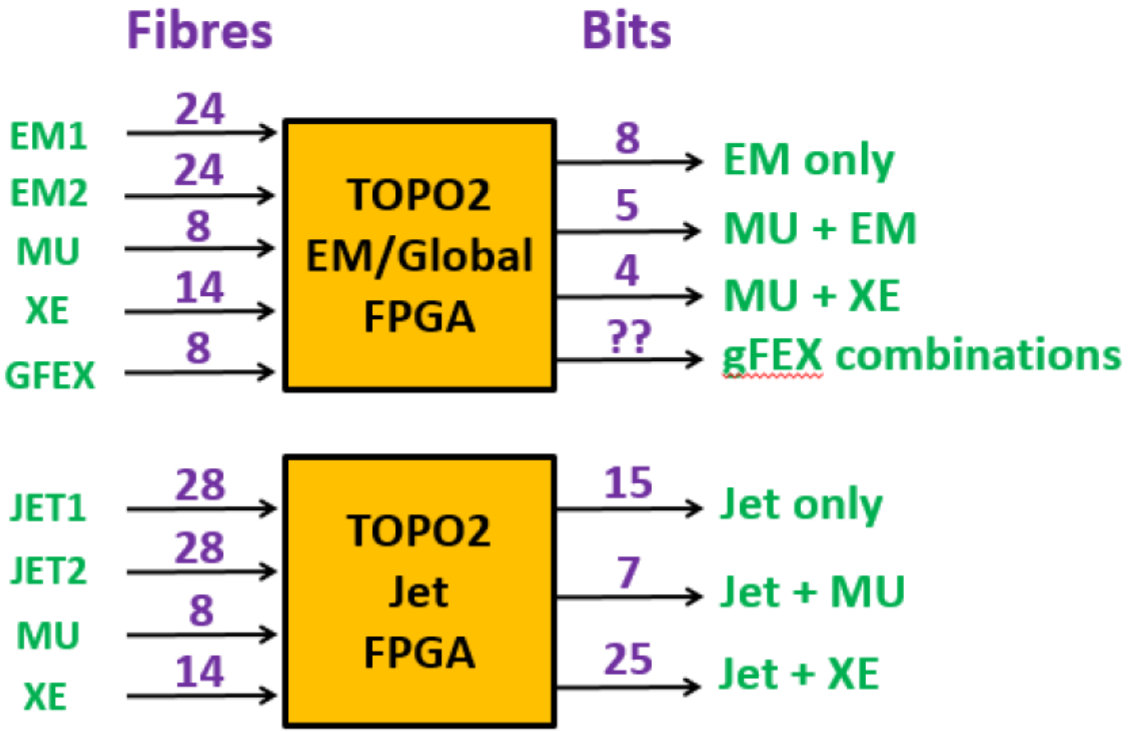
- Pure multiplicities
  - Replaces CMX
- Includes new gFEX outputs
- Simple, fast, parallel algorithms
- (No Muon inputs or outputs)
- Fits into current Topo design
  - In terms of i/o



How to get data into L1Topo (2)

TOPO2 Module: small topological combinations

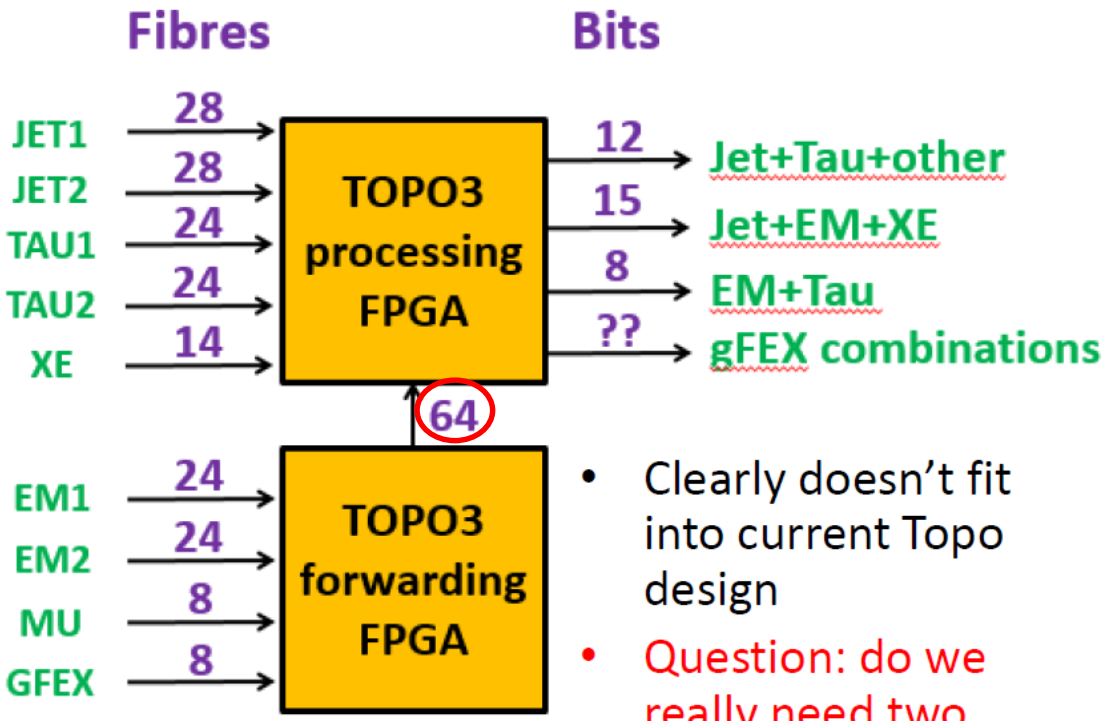
- Mostly single and double TOB type triggers
- Allows gFEX equivalent of JET triggers
- No Inter-FPGA communication



How to get data into L1Topo (3)

TOPO3 Module: Multi-TOB combinations

- ALL TOB types combined in one place!
- Huge input requirement for one FPGA
- Better separation possible but…
- A Jet+Tau+EM algorithm alone requires 152 links



- Clearly doesn't fit into current Topo design
- Question: do we really need two fibres for Jet/EM/Tau TOBs

L1Topo input bandwidth

- Current design is providing maximum bandwidth achievable with current technology
- TOPO3 module "need it all" won't work
- requiring inter-FPGA bandwidth above 600 Gb/s
- FPGAs have a maximum of ~200 Gb/s bandwidth in terms of parallel I/O.
- Additional latency on inter-FPGA links is an issue anyway

→ Need to work out what data are actually required in trigger combinations with all/many TOB types.

Work ongoing

Status of h/w development

- New L1Topo is jFEX based
- jFEX shown to work well in current incarnation (1 FPGA)
- jFEX programme ongoing ... Prototyping … review… preproduction…

- Real work:
  transformation jFEX → L1Topo can start soon (B.B.)

- Paper work:
  Engineering specs meant to be available April, 2017 – slight delay…

Backup slides

Latency at Phase-1

Table 13: L1Topo

	ns	BCs	Sub Total	Total	
Optical Input available from CMX, eFex, jFex & Muctpi				64,9	
L1Topo Input Deserialisers	50	2,0			
Synchronize to local clock - 320-> 40 MHz	25	1,0			
Algorithmic Processing	125	5,0			
			8,0		
Electrical Output to CTP (multiplexed) (if us	25	1,0			
Electrical Cable to CTP (if used) (2m)	10	0,4			
			1,4		
L1Topo electrical input available at CTP				74,3	L1Topo_Electrical
Output Multiplexers 40-320 MHz (if used)	25	1,0			
Output Serialisers for optics (if used)	50	2,0			
Fibres to CTP (if used) (2m)	10	0,4			
			3,4		
L1Topo Optical inputs to CTP available			11,4	76,3	L1Topo_Optical

L1Topo:

TDR figures

- Latency is tight
- Inter-FPGA fan-out is part of algo latency ! ~2BC ?
- Incoming signals on latency critical path (Muons / NSW) might bypass inter-FPGA fan-out (upstream duplication)
- Check input MGT/deserialization latency assumptions against current reality (Topo I)
- Electrical fast output path available (limited bandwidth)

Phase-2

- Seems that old plans for forward compatibility to Phase-2 have become obsolete.
- Therefore no Phase-2 slides in this presentation
- However, please note that there is plenty of optical output bandwidth available (up to 600Gb/s per L1Topo module) which is certainly not required into a Phase-1 style CTP.
- So probably well prepared for a new lease of life at Phase-2