Installation and Commissioning Plans for the jFEX

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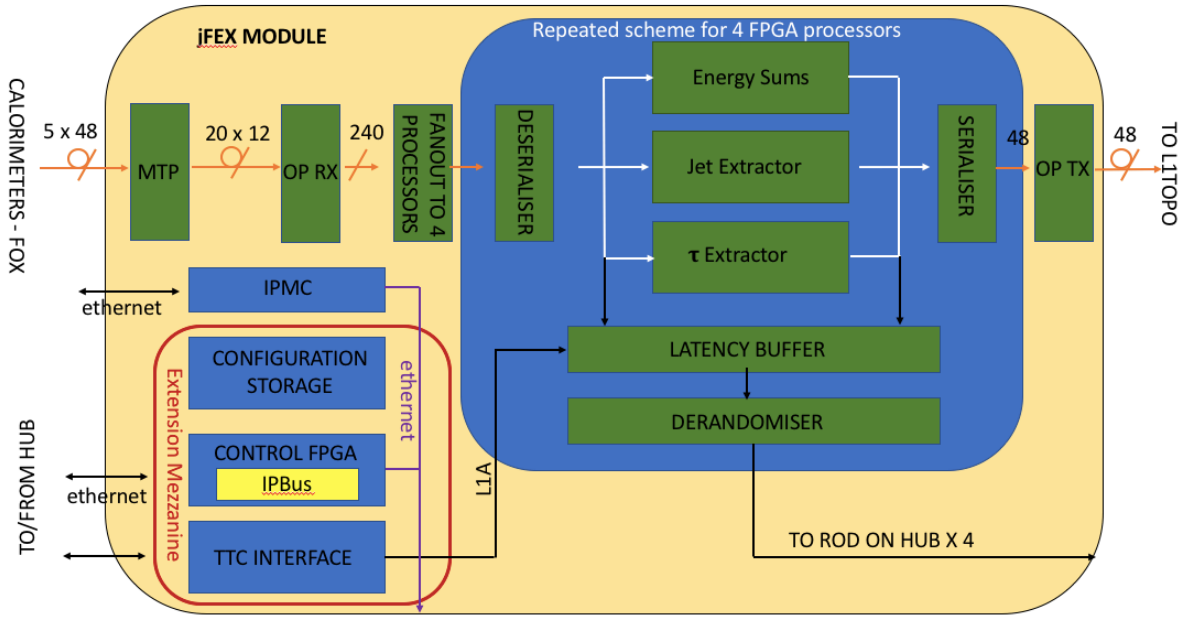
Agenda

- Introduction
- jFEX Status
- Hardware Availability
- Surface Test Facility
- Installation
- Commissioning
- Summary

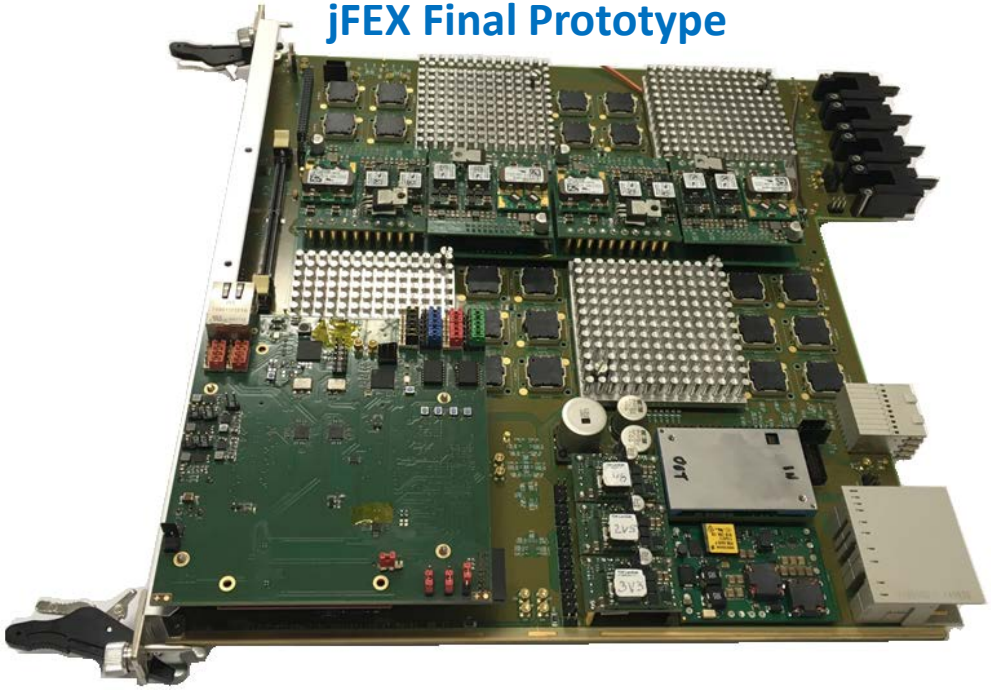
Introduction

- jFEX identifies jet candidates and calculates ΣE_T and E_T^{miss} for each BC
- $|\eta|< 4.9$ with different granularities
- 6 modules to be built
- Hardware details
  - ATCA board
  - 4 Xilinx UltrascalePlus FPGAs per module
    - XCVU9P-2FLGA2577E
    - Up to 120 MGTs per FPGAs
  - 24 MiniPOD: 20 RX + 4 TX
  - Modular design
  - Mezzanines
    - Power
    - Control

jFEX functionality – Block Diagram



jFEX Status


jFEX Final Prototype

- Final Design Review took place end of May
  - Firmware: May 29
    - https://indico.cern.ch/event/728398/
  - Hardware: May 30
    - https://indico.cern.ch/event/728400/
- Green light for producing the jFEX Pre-Production modules on June 12
- Ongoing PCB production
- Order of all components placed
- Expect delivery from assembly company: beginning of October
- Firmware
  - Ongoing integration of infrastructure firmware (MGTs, board control, IOs and etc.) and algorithms

Hardware Availability (Plan)

- jFEX First Prototype – Currently at CERN (STF)
  - Equipped with one UltraScale FPGA
- jFEX Final Prototype – Currently in Mainz
  - Equipped with four UltraScale+ FPGAs
- jFEX Pre-Production Module – Available from November 2018 onwards
  - Pre-Production module will be used as spare
- jFEX Production Modules – Available from May 2019 onwards
  - 9 (+ 1) modules
    - 6 to be installed
    - 3 (+ 1) spares

Surface Test Facility (1)

Final Prototype = Pre-Production Module = Production Module

- No hardware changes are foreseen from prototype to production module
- Initial integration tests with other systems can start at anytime with Final Prototype
  - And with Pre-Production by November
- Combined tests with TREX schedule for beginning of September (in Heidelberg)
- Combined tests with ROD (Hub) to take place soon

Surface Test Facility (2)

- Setup ready for tests with jFEX First Prototype and FTM since July
  - Tests of optical links, TTC clock reception, IPBus and etc. were performed
  - jFEX Final Prototype is currently in Mainz, but will be shipped back to CERN soon
- What can and cannot be done elsewhere?
  - Will we be able to perform tests with some calorimeter boards?
  - How/what will be the DCS setup on the STF?

jFEX setup on the STF

Surface Test Facility
Pre-Production Module

- Validation of Pre-Production module will take place at the STF
    - Smoke tests and basic validation of board optical/electrical links (IBERT) to be done in Mainz
  - Validation of all optical/electrical inputs/outputs simultaneously (IBERT and formatted data)
  - Power consumption
    - Ripple measurement
    - Thermal dissipation
  - LHC clock reception
    - MGTREF clock jitter measurement
  - Validation of the backplane high-speed links
    - Readout and TTC data
    - Latency measurement
    - IPMC
- Firmware consolidation
  - Tests with integrated firmware (infrastructure and algorithms)
  - Latency measurement
  - Combined tests with other parts of the system

Surface Test Facility
Production Module

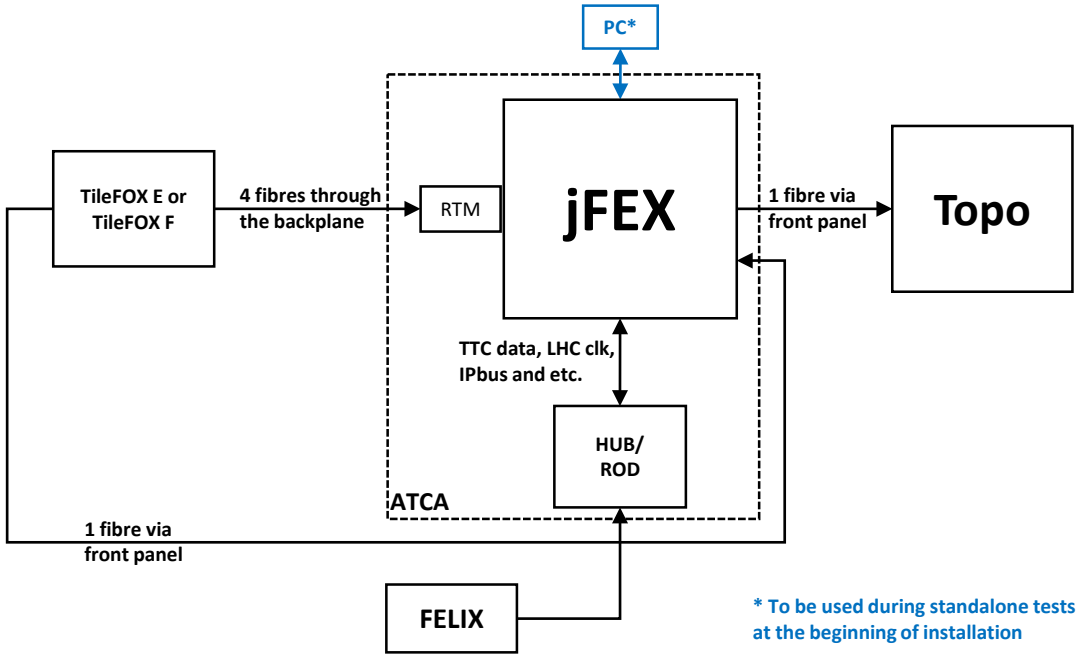
- Initial production modules acceptance tests will take place in Mainz
  - Smoke tests and basic validation of board optical/electrical links (IBERT)
- Finalization of production modules acceptance tests on ATCA crate with HUB/ROD and/or FTM
  - Same test list of the Pre-Production module
- Full slice test from Latome/TREX via jFEX to Topo
  - As much as possible inputs
    - Formatted data
  - With all possible infrastructure parts
    - Hub/ROD, FELIX, IPBus, DCS and etc.
  - Final evaluation on power consumption and cooling with closed shelf
- Integration with “L1Calo STF partition”

USA15 Installation (1)

- jFEX connections
  - LATOME
  - TREX
  - FOX
  - Hub/ROD
    - FELIX
  - Topo
    - Installation schedule for December 2019

To be defined?

To be installed before jFEX



- Initial tests
  - Verification of board functioning after transport
  - Establishment of board communication and control
    - IPbus and DCS
  - Integration tests with HUB/ROD
  - Combined tests with calorimeters

Ideally, similar to what was done in STF during 2018 and 2019

USA15 Installation (2)

- Starts in November 2019
  - Followed by 3 months re-integration & commissioning
  - What is the installation sequence?
    - Will the crate be already in USA15?
      - With all FOX connections done?
    - Or will it be transported from the STF with all boards?
    - When will the Hub/ROD be installed?
  - Will we take care of transportation and fibre connection ourselves?
  - Should we perform tests with the Prototype/Pre-Production module in USA15 before installation?

Commissioning

- Validation of (FOX) input mapping
- Integration with ATLAS partition
- Online monitoring
- Combined tests with calorimeter
- Timing calibrations
- Pre-beam commissioning with cosmics
- Commissioning with beam
- Validation with bit-wise simulation
- Cross-comparison with legacy system

Summary

- Ongoing production of the jFEX Pre-Production module
- Pre-Commissioning to take place during 2018 and 2019 at the STF
  - Setup ready on the STF for jFEX
  - Finalization of production modules acceptance tests
- Installation in USA15 scheduled for November 2019

jFEX Schedule

Task Name	Start	Finish	Duration	Predecessors
jFEX	Thu 17/01/13	Fri 07/06/19	1637 dys	
Project management	Thu 17/01/13	Wed 04/04/18	67 mons	
Prototype	Thu 17/01/13	Fri 26/05/17	1127 dys	
Prototype 2	Mon 29/05/17	Fri 25/05/18	250 dys	61
Pre-Production	Mon 28/05/18	Fri 18/01/19	160 dys	
Final Design Review	Mon 28/05/18	Fri 22/06/18	4 wks	65
Manufacture of Prod. PCBs +	Mon 25/06/18	Fri 05/10/18	15 wks	67
Tests	Mon 08/10/18	Fri 30/11/18	8 wks	68
Contingency	Mon 03/12/18	Fri 18/01/19	5 wks	69
Production	Fri 18/01/19	Fri 07/06/19	100 dys	
Production Readiness Review	Fri 18/01/19	Fri 18/01/19	0 dys	70
Assembly	Mon 21/01/19	Fri 15/02/19	4 wks	72
Acceptance Tests	Mon 18/02/19	Fri 12/04/19	8 wks	73
Contingency	Mon 15/04/19	Fri 07/06/19	8 wks	74
Firmware	Mon 01/02/16	Fri 26/10/18	695 dys	
Algorithm	Mon 01/02/16	Fri 22/12/17	97 wks	
MGT Basic Infrastructure	Mon 06/03/17	Fri 31/03/17	4 wks	
IPBus Prototype Firmware	Mon 06/03/17	Fri 31/03/17	4 wks	
Module Control	Mon 02/10/17	Fri 26/10/18	270 dys	
I2C Control	Mon 20/11/17	Fri 26/10/18	47 wks	
Basic Monitoring & Diagnc	Mon 02/10/17	Fri 22/12/17	12 wks	
Real-Time Path Control To	Mon 02/10/17	Mon 02/10/17	1 dy	
Configuration	Mon 30/10/17	Fri 26/10/18	50 wks	
IPMC	Mon 02/10/17	Fri 12/10/18	52 wks	
Readout: Specification	Wed 12/07/17	Tue 05/09/17	8 wks	
Readout: Implementation	Wed 06/09/17	Fri 27/07/18	223 dys	86
Readout: Testing	Mon 30/07/18	Fri 14/09/18	35 dys	87
Tests with Playback	Mon 30/07/18	Fri 03/08/18	1 wk	87
Integrating with RTDP	Mon 30/07/18	Fri 14/09/18	7 wks	87
Integrating with IPBus	Mon 30/07/18	Fri 07/09/18	6 wks	87
Integrating with Hub	Mon 30/07/18	Fri 24/08/18	4 wks	87
System tests	Mon 29/05/17	Fri 18/01/19	20.5 mons	61