jFEX / L1Topo

– Status & Plans (medium term) –

Uli / MZ
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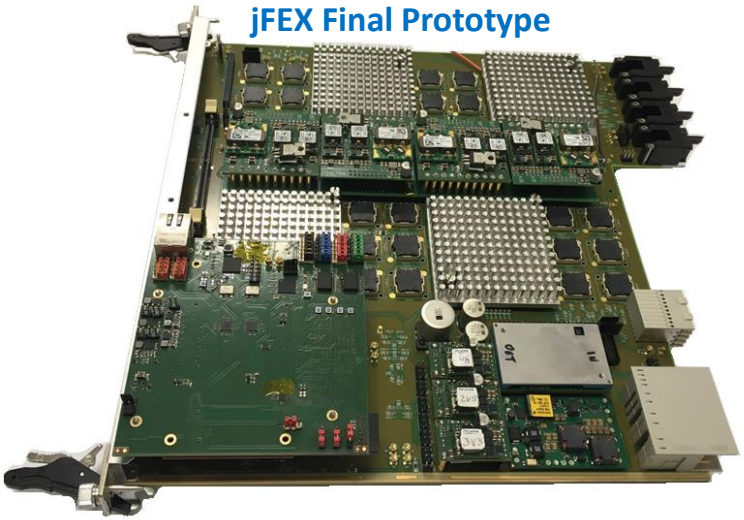
jFEX Status


jFEX Final Prototype

- Pre-Production module
  - Ordered full set of production PCBs (10 pieces), because of no significant cost impact
  - Delay at PCB manufacturer, because of long lead time of PCB material
  - PCBs at assembly company
  - Assembly (SMT) being worked on
  - Some components (THT) were difficult to procure, going out to assembly company today. THT components last assembly step anyway.
  - Expect to have the board in Mainz early December
  - Tests of Pre-Production board will be only verification along the lines of prototype tests
    - No design changes wrt Final Prototype
  - All components for final production in hands, therefore **NO** further **DELAYS** expected at next stage…
- Firmware
  - Ongoing integration of infrastructure firmware (MGTs, board control, IOs and etc.) and algorithms

Hardware Availability (Status/Plan)

- jFEX First Prototype – Currently at CERN (STF)
  - Equipped with one UltraScale FPGA
- jFEX Final Prototype – Currently at CERN (STF)
  - Equipped with four UltraScale+ FPGAs
- jFEX Pre-Production Module – Available from mid December 2018 onwards
  - Pre-Production module will be used as a spare, once production modules have been built
- jFEX Production Modules – Available from May 2019 onwards
  - 9 (+ 1) modules
    - 6 to be installed
    - 3 (+ 1) spares

Module tests

Final Prototype = Pre-Production Module = Production Module

- No hardware changes are expected from prototype through production modules
- Rigorous tests of first and final prototype taken place
  - in Mainz (power-up, local loopback IBERT, power drain / thermal tests)
  - In Heidelberg (TREX link tests, IBERT, in September)
  - At **STF** (see next slide)
- Final Prototype **available** for system-level tests (integration tests)
- Pre-Production from December/ January

Surface Test Facility

- Setup ready for tests with jFEX First Prototype and FTM since July
  - Tests of optical links, TTC clock reception, IPBus and etc. were performed
  - jFEX Final Prototype was shipped to CERN along with L1Topo prototype. Initial tests done.
- Joint test week for jFEX final prototype ≡ Pre-Production and L1Topo with **software/firmware integration** in week Dec. 10
- Expecting to run formatted data jFEX→L1Topo

jFEX setup on the STF

Next tests @ STF

System-level tests with all interfacing modules

- jFEX and L1Topo (prototype) meant to be at the STF long-term, joint tests possible over long periods . Starting wk. Dec. 10.
- IPbus being exercised during all tests
- DCS – make use of it as it becomes available. Initial steps (test wk. Dec. 10):
  - Read some environmental conditions via IPbus
  - Start using IPMC for reading some basic I2C sensor data
- Initial readout tests with Hub/ROD planned for wk. Dec. 10 (Marek)
- Start LATOME → jFEX integration asap
- Need to discuss LATOME availability and required tests pre-PRR

NEED TO SCHEDULE TESTS WITH THE RESPECTIVE MODULES

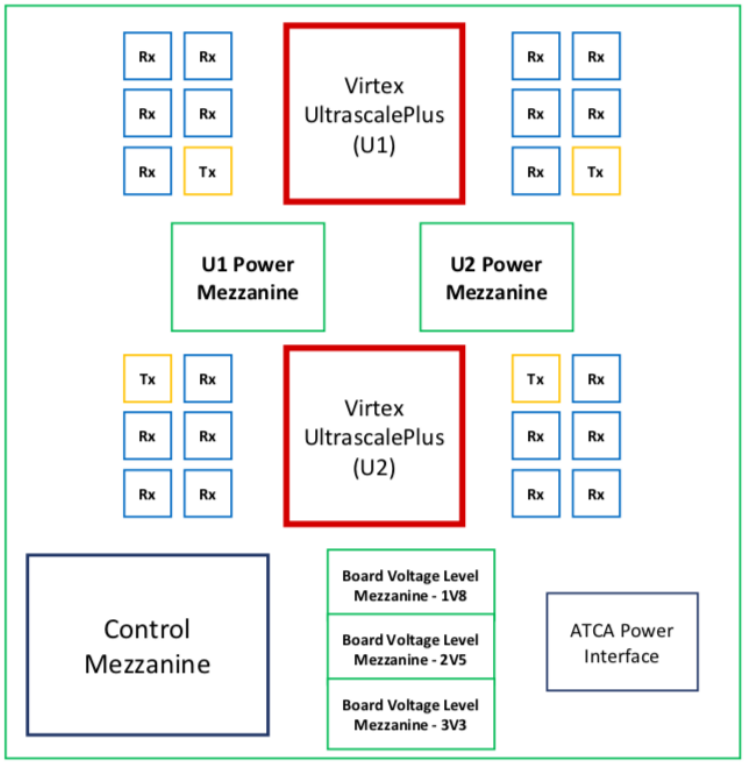
Production modules

- Expect to get through volume production quickly: No more delays due to component procurement issues
- As soon as we get the go-ahead, assembly can start

- Bruno expecting to complete ~ 2 modules per week
- Going through established test routine in Mainz won‘t take much time
- → expect the production modules to populate the STF quickly once we are through the PRR

AGAIN, NEED TO SCHEDULE TESTS

- L1Topo based on jFEX hardware-wise
  - 2 Ultrascale+ FPGAs per module
  - 118 input fibres per processor FPGA (6.4, 11.2 and 12.8 Gb/s)
  - 24 output fibres per processor FPGA (6.4 and 12.8 Gb/s)
- Inter-FPGA connectivity 64 Gb/s (latency!)
- Control on mezzanine
- Electrical and optical output to CTP
- 3 ATCA modules at Point 1



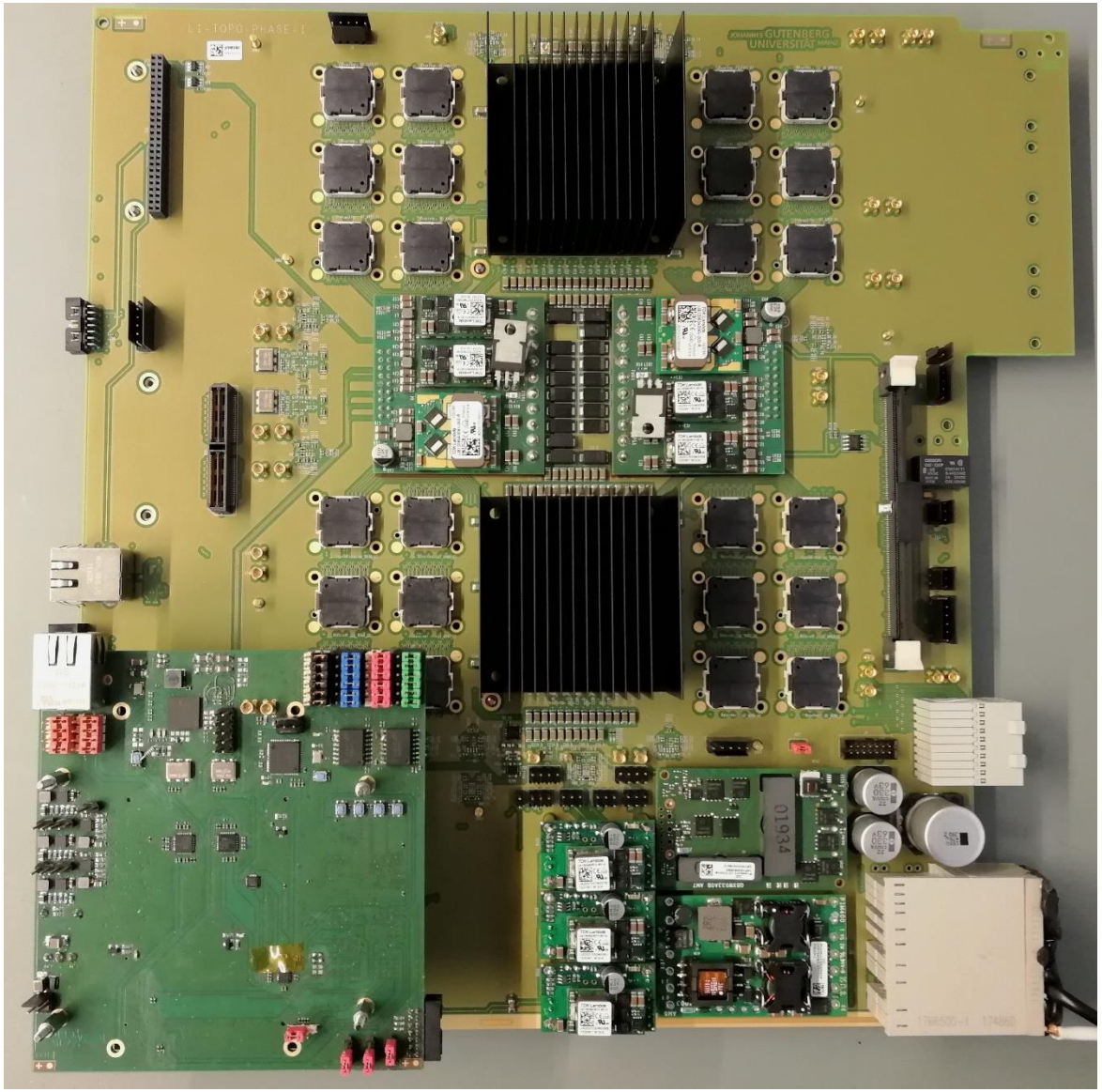
Prototype at CERN since end of October `18

L1Topo prototype

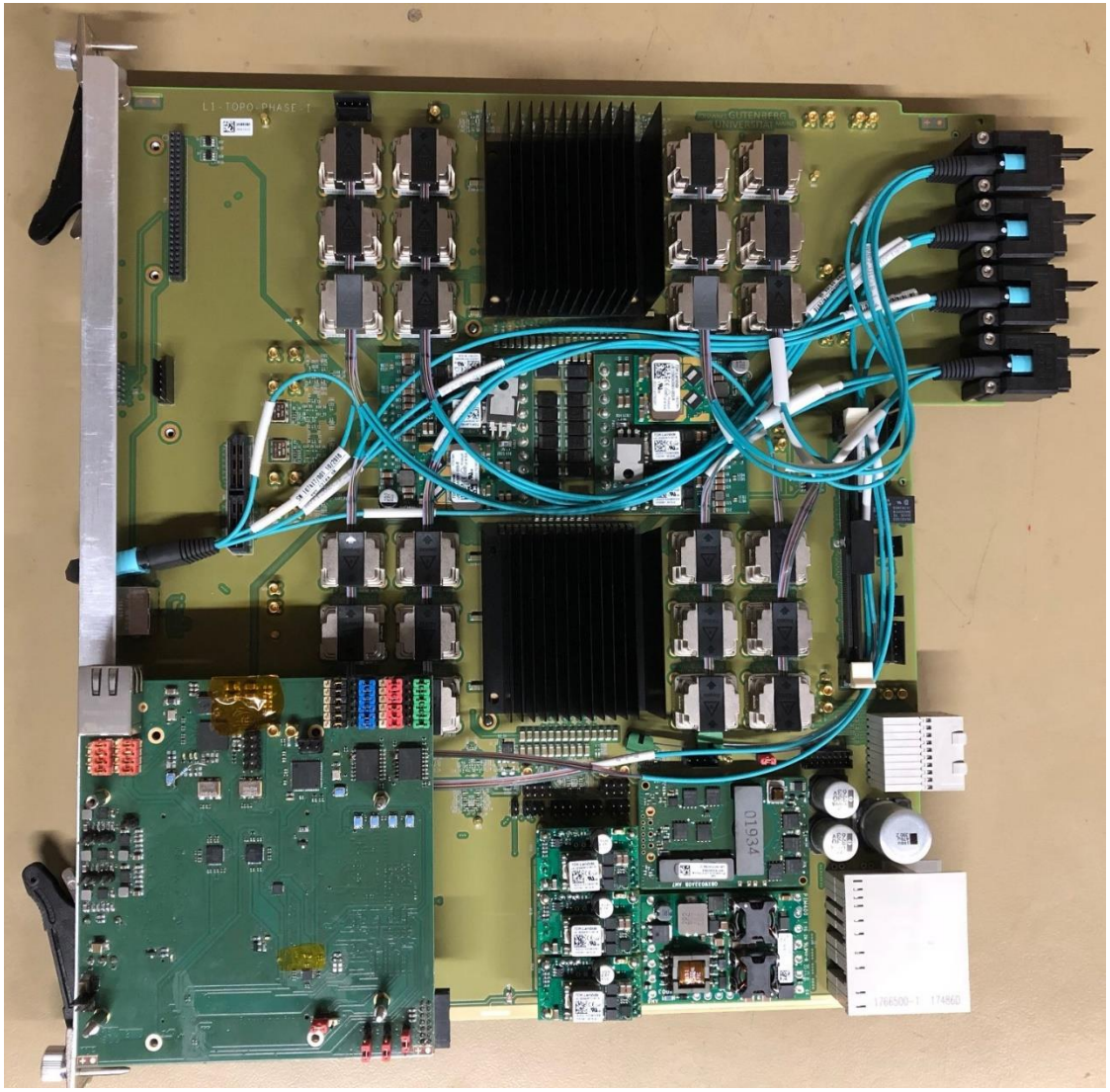
In Mainz…

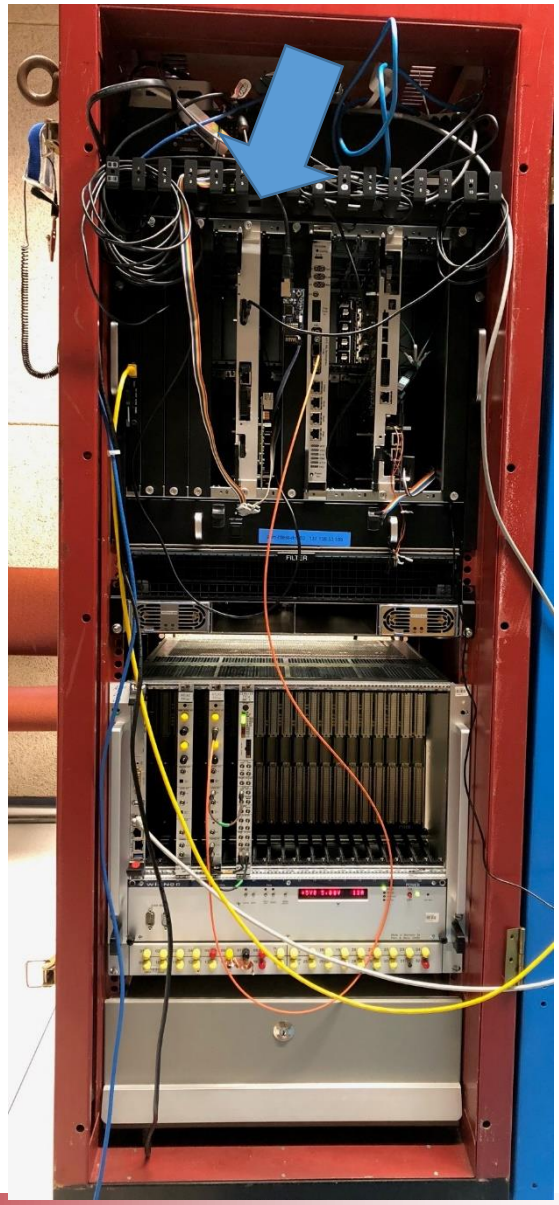
… initial smoke tests…

..without optics…



Fibred… and at STF finally …





L1Topo Status

- Preliminary design review took place in November 2017

  https://indico.cern.ch/event/676491/
- L1Topo currently at STF for testing together with the jFEX final prototype
- Final design review scheduled on January 23rd 2019
- Firmware
  - Ongoing integration of infrastructure firmware (MGTs, board control, IOs and etc.) and algorithms

Surface Test Facility (1)

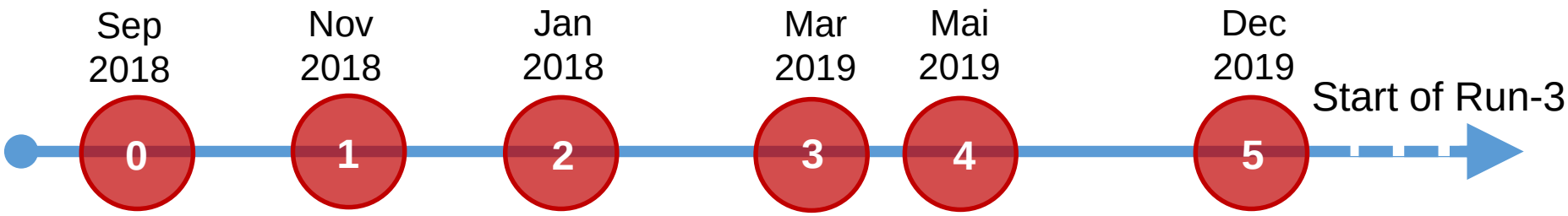
Final Prototype = Pre-Production Module = Production Module

- No hardware changes are foreseen from prototype to production module
- Initial integration tests with other systems can start at anytime with prototype
- Combined tests with jFEX already ongoing
  - Scheduled dedicated test week for software and firmware mid of December with all experts present
- Combined tests with eFEX, gFEX, MUCTPI and CTP still need to be scheduled

Surface Test Facility (2)

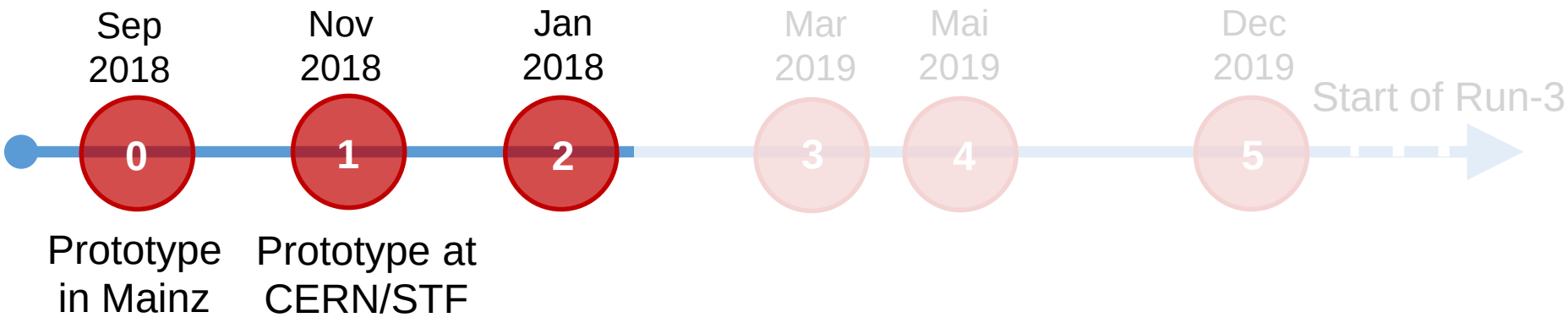
- Setup ready for tests with L1Topo prototype, jFEX and FTM since beginning of November
  - Tests of optical links, TTC clock reception, IPBus and etc. were performed
- Aim to test and validate full module functionality at STF **except**:
  - **Concurrent** operation of all FEXes (all modules), MUCTPI and CTP
  - Validation of input mapping
  - Final timing calibration

Major Milestones for L1Topo towards Installation



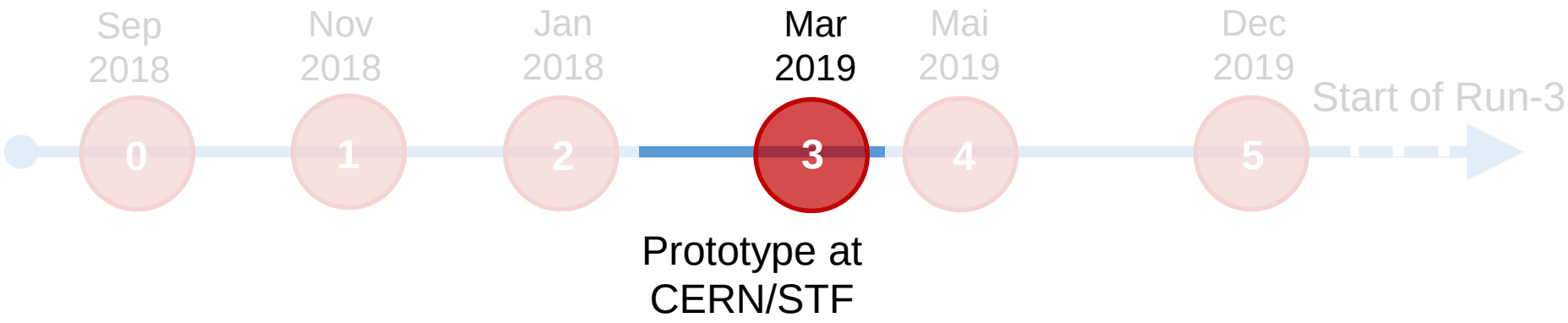
- 0 Prototype in Mainz
- 1 Prototype available at CERN/STF
- 2 Final Design Review
- 3 Production Readiness Review
- 4 Production modules available at CERN/STF
- 5 Installation in USA15

Prototype at STF/CERN



- Initial validation tests of prototype has been done in Mainz
  - Smoke tests and basic validation of board optical/electronical links
- Prototype available at CERN since end of October 2018
- Validation of prototype currently ongoing at STF/CERN
  - Integrated test with FTM and jFEX
  - Validation of all input and output links concurrently
  - TTC and ROD links
  - Latency measurement
  - I2C/IPBus/OPC/DCS tests
  - Power tests with all interfaces fully active
- FDR scheduled for January 23rd 2019

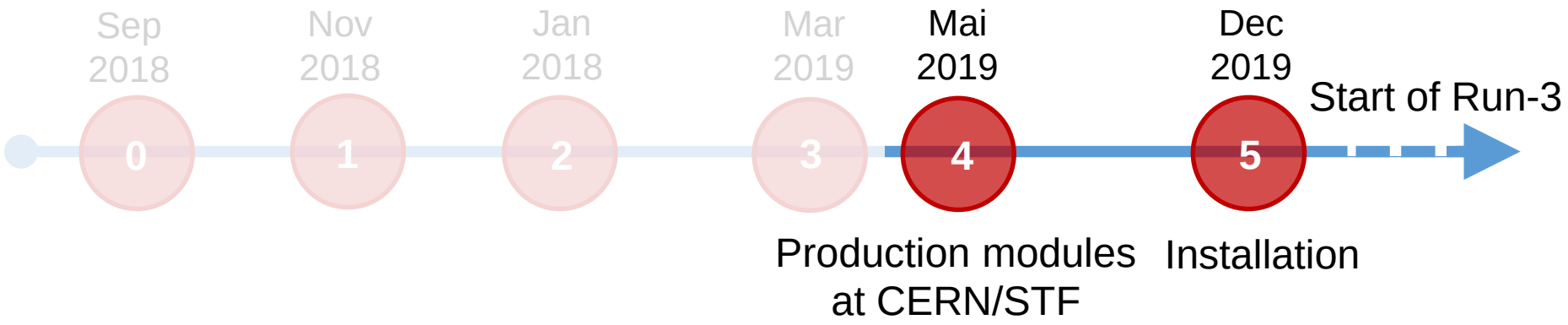
Prototype/**Preproduction** @ STF/CERN



Final Prototype = Pre-Production Module = Production Module

- Continue validation of prototype/pre-production module at STF/CERN
  - Integrated test with FTM, FEXes, MUCTPI and CTP
- Aim for PRR end of March 2019

Production modules at STF/CERN



- Initial acceptance tests will be done in Mainz
  - Smoke tests and basic validation of board optical/electronical links
- Production modules will be available at CERN Mai 2019
- Finalization of acceptance tests on ATCA crate in the STF
- Full slice test with all FEXes via Topo to CTP
- Integration with „L1Calo STF partition“
- Final installation steps planned for December 2019 to maximize time for pre-commissioning at STF
  - Followed by 3 month re-integration & commissioning

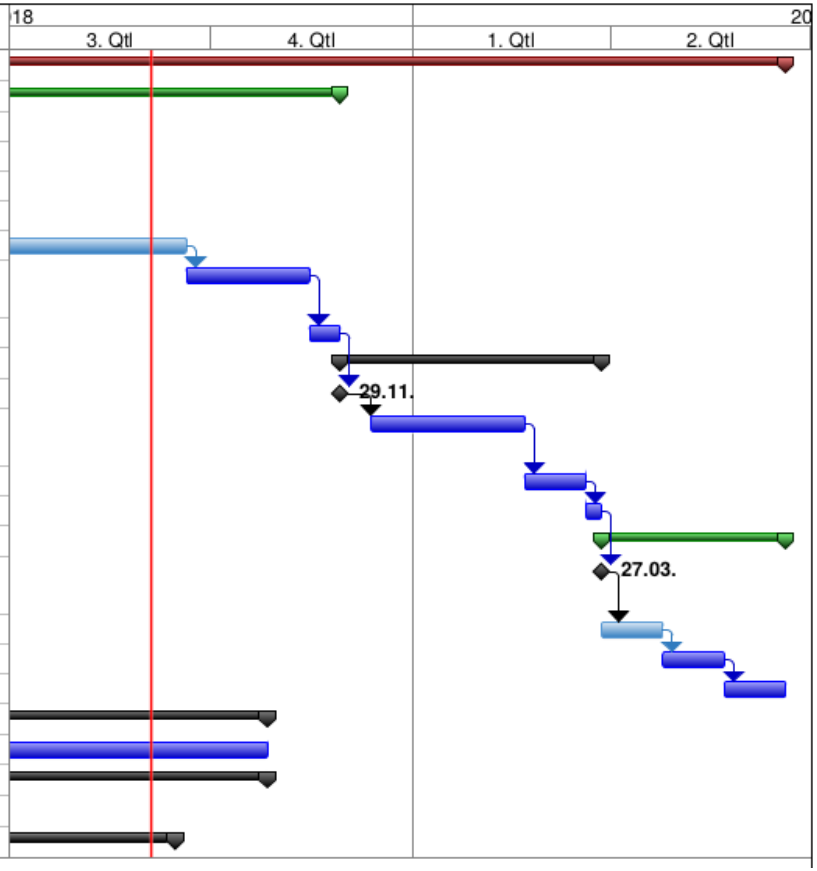
Summary

- jFEX and L1Topo prototypes at CERN / STF
  - Integrated tests currently ongoing
  - System level tests starting wk Dec. 10
  - L1Topo FDR planned for January 23rd 2019
- L1Topo Production modules available at STF/CERN Mai 2019 (Schedule includes 7 weeks contigency)
- Work towards final installation steps Dec. 2019

Back-Up

Phase-1 L1Topo Schedule

Nr.	Task Name	Anfang	Fertig stellen	Dauer
94	**Phase-I L1Topo**	**Mo 09.01.17**	**Mi 19.06.19**	**618 Tage**
95	**Prototype**	**Mo 09.01.17**	**Mi 28.11.18**	**483 Tage**
96	Engineering specification	Mo 09.01.17	Fr 18.08.17	32 Wochen
97	Preliminary Design Review	Fr 10.11.17	Fr 10.11.17	0 Tage
98	Schematic Entry	Mo 21.08.17	Fr 24.11.17	14 Wochen
99	Layout + PCB Simulation	Mo 27.11.17	Fr 18.05.18	23 Wochen
100	Manufacture + Assembly	Mo 21.05.18	Mi 19.09.18	88 Tage
101	Acceptance and Integrated Tests	Do 20.09.18	Mi 14.11.18	8 Wochen
102	Contingency	Do 15.11.18	Mi 28.11.18	2 Wochen
103	**Pre-Production**	**Do 29.11.18**	**Mi 27.03.19**	**75 Tage**
104	Final Design Review	Do 29.11.18	Mi 12.12.18	2 Wochen
105	Manufacture of Prod. PCBs + Assembly of Pre-Prod.	Do 13.12.18	Mi 20.02.19	8 Wochen
106	Tests	Do 21.02.19	Mi 20.03.19	4 Wochen
107	Contingency	Do 21.03.19	Mi 27.03.19	1 Woche
108	**Production**	**Mi 27.03.19**	**Mi 19.06.19**	**60 Tage**
109	Production Readiness Review	Mi 27.03.19	Mi 27.03.19	0 Tage
110	Assembly	Do 28.03.19	Mi 24.04.19	4 Wochen
111	Acceptance Tests	Do 25.04.19	Mi 22.05.19	4 Wochen
112	Contingency	Do 23.05.19	Mi 19.06.19	4 Wochen
113	**Firmware**	**Mo 21.08.17**	**Fr 26.10.18**	**300 Tage**
114	Algorithm	Mo 21.08.17	Fr 26.10.18	60 Wochen
115	**Control**	**Mo 21.08.17**	**Fr 26.10.18**	**300 Tage**
120	**Real-Time Data Path**	**Mo 21.08.17**	**Fr 23.03.18**	**145 Tage**
124	**Readout**	**Mo 21.08.17**	**Fr 14.09.18**	**270 Tage**



jFEX Schedule

Task Name	Start	Finish	Duration	Predecessors
jFEX	Thu 17/01/13	Fri 07/06/19	1637 dys	
Project management	Thu 17/01/13	Wed 04/04/18	67 mons	
Prototype	Thu 17/01/13	Fri 26/05/17	1127 dys	
Prototype 2	Mon 29/05/17	Fri 25/05/18	250 dys	61
Pre-Production	Mon 28/05/18	Fri 18/01/19	160 dys	
Final Design Review	Mon 28/05/18	Fri 22/06/18	4 wks	65
Manufacture of Prod. PCBs +	Mon 25/06/18	Fri 05/10/18	15 wks	67
Tests	Mon 08/10/18	Fri 30/11/18	8 wks	68
Contingency	Mon 03/12/18	Fri 18/01/19	5 wks	69
Production	Fri 18/01/19	Fri 07/06/19	100 dys	
Production Readiness Review	Fri 18/01/19	Fri 18/01/19	0 dys	70
Assembly	Mon 21/01/19	Fri 15/02/19	4 wks	72
Acceptance Tests	Mon 18/02/19	Fri 12/04/19	8 wks	73
Contingency	Mon 15/04/19	Fri 07/06/19	8 wks	74
Firmware	Mon 01/02/16	Fri 26/10/18	695 dys	
Algorithm	Mon 01/02/16	Fri 22/12/17	97 wks	
MGT Basic Infrastructure	Mon 06/03/17	Fri 31/03/17	4 wks	
IPBus Prototype Firmware	Mon 06/03/17	Fri 31/03/17	4 wks	
Module Control	Mon 02/10/17	Fri 26/10/18	270 dys	
I2C Control	Mon 20/11/17	Fri 26/10/18	47 wks	
Basic Monitoring & Diagnc	Mon 02/10/17	Fri 22/12/17	12 wks	
Real-Time Path Control To	Mon 02/10/17	Mon 02/10/17	1 dy	
Configuration	Mon 30/10/17	Fri 26/10/18	50 wks	
IPMC	Mon 02/10/17	Fri 12/10/18	52 wks	
Readout: Specification	Wed 12/07/17	Tue 05/09/17	8 wks	
Readout: Implementation	Wed 06/09/17	Fri 27/07/18	223 dys	86
Readout: Testing	Mon 30/07/18	Fri 14/09/18	35 dys	87
Tests with Playback	Mon 30/07/18	Fri 03/08/18	1 wk	87
Integrating with RTDP	Mon 30/07/18	Fri 14/09/18	7 wks	87
Integrating with IPBus	Mon 30/07/18	Fri 07/09/18	6 wks	87
Integrating with Hub	Mon 30/07/18	Fri 24/08/18	4 wks	87
System tests	Mon 29/05/17	Fri 18/01/19	20.5 mons	61