IPbus / Flash configurator

(pre) History and some technical details:

- Processor configuration (stacked, huge) SPI memories located on eXtension mezzanine
- **Golden image** configuration scheme already tried out on jFEX, ~April, 2018 – using JTAG access
- Including verification for bitfiles spanning die boundaries
- For a little while already, we have had an IPbus slave, capable of reading/writing flash memories on KC705 eval board.

In 2019:

- Port that piece of VHDL code (IPbus slave only) to eXtension mezzanine (i.e. target a Zynq device) and include into existent IPbus infrastructure
- Write accompanying control software
- Results: **Writing: ok, reading: ok**, standalone verification CRC64/ECMA yet to be completed
- Development got delayed for a bit due to occasional packet losses and the need for **soak tests**
- Successfully tested at very last minute before review:
  100 Million IPbus operations (UDP) / **no error**, as of today

  → The mezzanine **hardware is ok**, no issues with the **improved PHY** scheme