Slice test – L1Topo

Goal: operate L1Topo real-time inputs with all FEXes and spy on the data

Executive summary: L1Topo operated with input data from all FEXes. Mostly success.

- Topo used during test week: new, production module
- Few fixes required:
  - Update Topo firmware to existent register model
  - Load .jed configuration file to CPLD
  - Sort out an issue with hub clocking (TTC vs. XTAL)
- Individual tests to confirm operation as of previous tests, and uncover remaining issues.
- Error counters checked
- Apparent clock synch issues confirmed/ruled out via (IBERT) recovered clock monitoring
- Data recorded in spy memories

L1Topo results

- gFEX – success
  - Clock synchronicity confirmed eventually
  - CRC scheme not compatible to the one used on L1Topo, as **expected**.
  - Data received in spy memories
- eFEX – partial success
  - Data received as sent out by eFEX
  - Clock synchronicity difficult to achieve. Possible cause for observed word alignment issues. TBD…
  - CRC couldn't be checked due to alignment issue
  - Lack of trailer word in case of zero TOBs unexpected feature (idle pattern instead in trailer word)
- Final slice test run with data taken concurrently from all three systems. Data sourced from TREX.
- Analysis/interpretation yet to be done

Need to discuss CRC scheme and eFEX idle pattern scheme, and clocking

Plans

- Integrate with algorithms
- Extend spy scheme to capture additional data (e.g. algorithm-internal data / sort of XTOBs)
- Integrate with readout circuitry

Try to achieve as much integration as possible before next slice test !