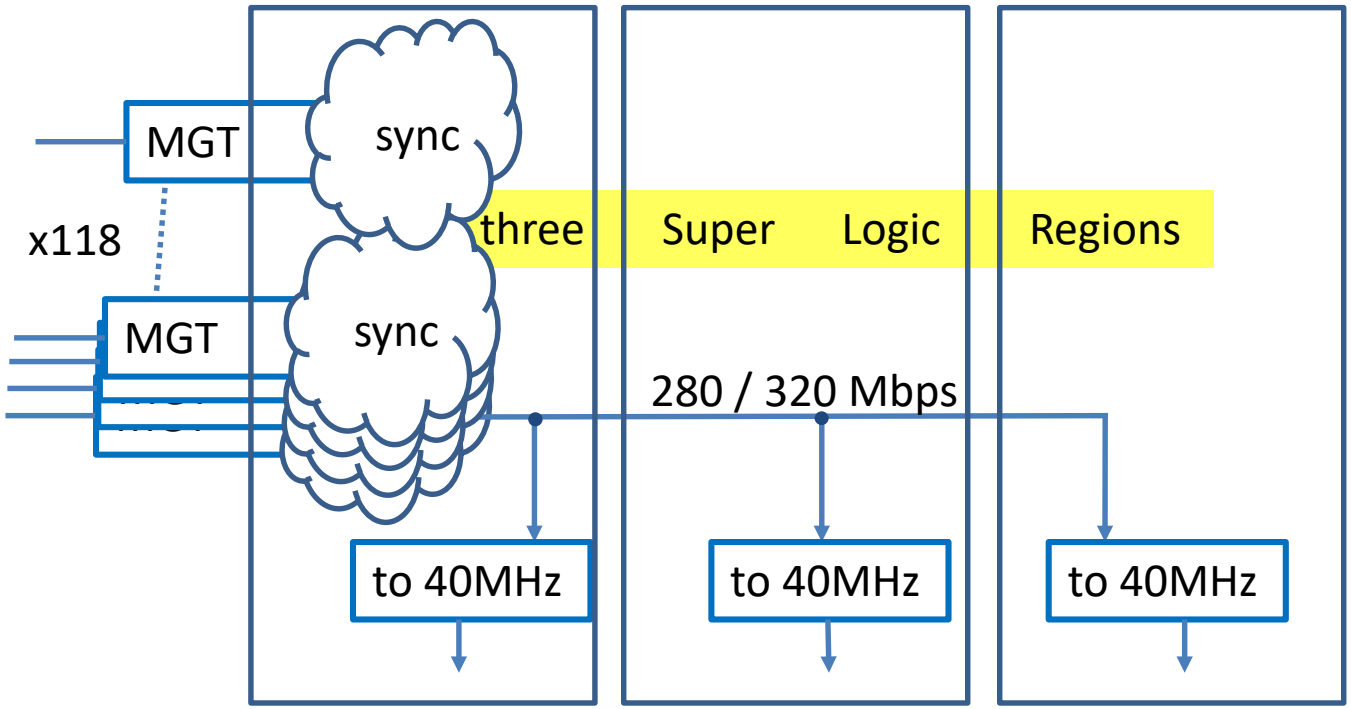
L1Topo and jFEX data reception f/w

- Incoming real-time data at 11.2Gbps (jFEX) / 11.2 & 12.8 (L1Topo)
- MGT-internal parallel data at per-channel word clock (280/320 MHz)
  - Up to 118 clock domains per FPGA → need to synchronize
  - Distribution of 118 clock domains over 3 SLRs "challenging"
  - Inter-SLR connectivity insufficient for fan-out at 40MHz

→Need to synchronize once, and replicate in global 280/320 MHz domain



L1Topo and jFEX data reception f/w

- That affects latency:
  - Requires synchronizer at MGT word rate
  - Need to pipeline SLR crossings
- Decided in favour of buffered MGT mode rather than sync in fabric
  - Higher latency than phase-alignment alone, but avoid fabric buffer
  - Well within previous latency estimates/envelope (Christian)