Slice test report – L1Topo

Goal (again): operate L1Topo real-time inputs with all FEXes and spy on the data

Executive summary (again): L1Topo operated with input data from FEXes. Mostly success:

- Individual tests to confirm operation as of previous tests, and uncover remaining issues.
- Formatted data tests
- Error counters checked
- Data recorded in spy memories for all FEXes
- Initial synch/alignment issues with both eFEX and gFEX
- Eventually properly aligned data received.
- CRC – not matching at receiving end
- Spy memory captured data provided to respective FEXes
- BCIDs seem to jump at gFEX received data
- Further analysis/interpretation been done ?

Preparations / plans

Before slice test week have a go at:

1. Integrate play/spy circuitry with TTC data to synchronize spy data to BCreset
2. Arrive at a near final mapping for interface between MGT infrastructure and algorithms (Christian, Johannes, Ralf)
3. Extend spy scheme to capture additional data (e.g. algorithm-internal data and L1A)
4. Integrate with readout circuitry (Marek)

Synched data transmission for full slice comes in two required steps:

1) With spy memory readout

4) With readout to ROD