L1Topo recent work / status / plans

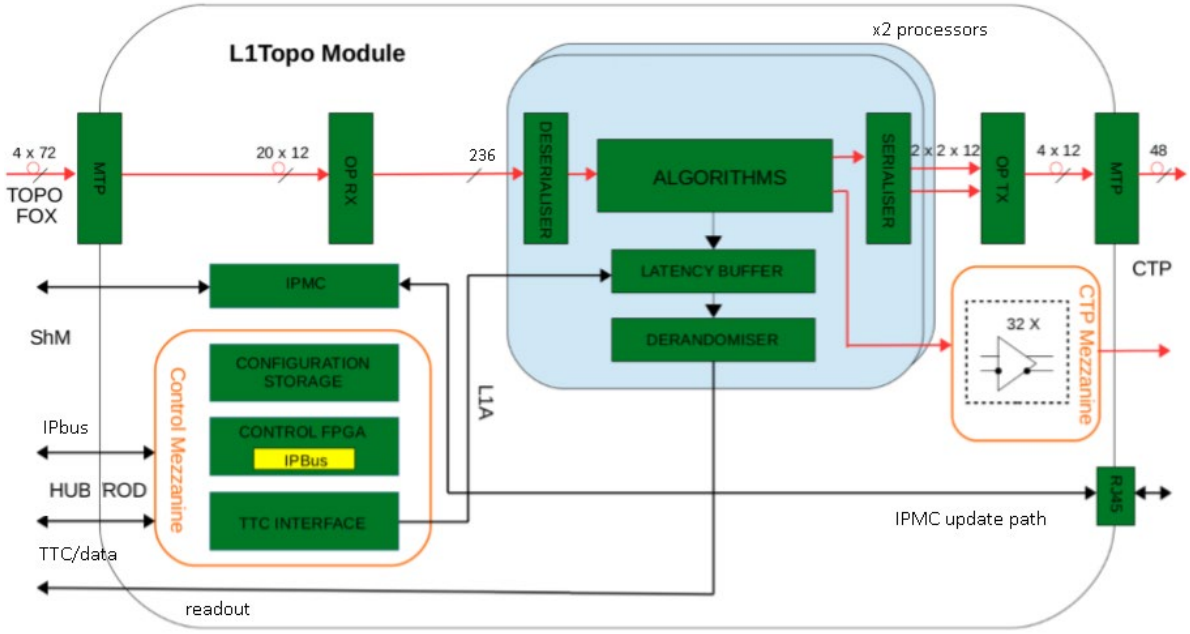
Uli, Julio / Mainz

Hardware
Firmware (infrastructure/control)
Tests

Hardware Overview

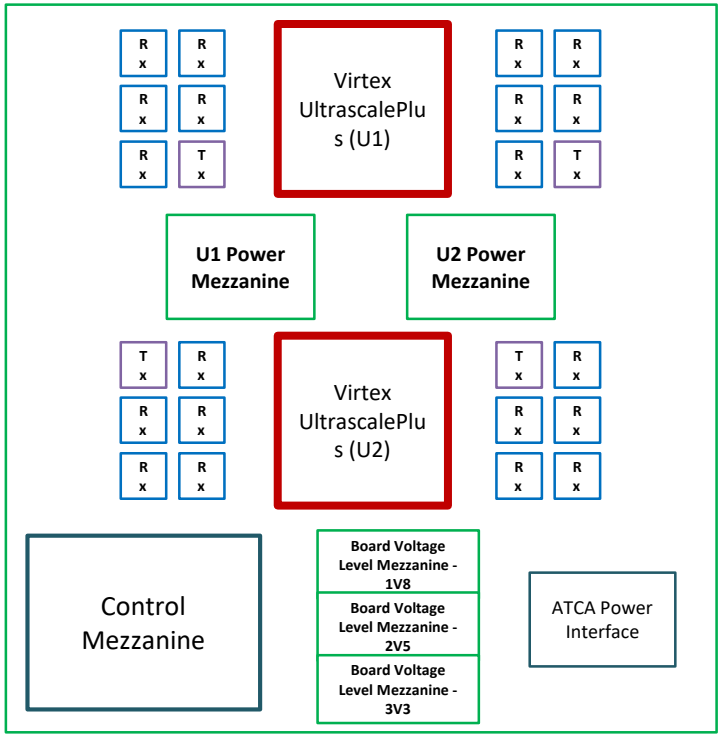
- ATCA board (based on jFEX design)
  - Modular design
- 2 Virtex UltrascalePlus FPGAs

- Two iterations
- Prototype (FDR 01/2019)
- Final design presented at PRR 08/2019
  - Fix on MGT calibration



Hardware Overview

- ATCA board (based on jFEX design)
  - Modular design
- 2 Virtex UltrascalePlus FPGAs
  - XCVU9P-2FLGA2577E
  - 120 MGTs (GTY) per FPGA
    - 118 input fibres per processor FPGA
- 24 MiniPOD: 20 RX + 4 TX
- Mezzanines
  - Control & Power
  - Both compatible with jFEX
  - CTP interface module (LVDS drivers)



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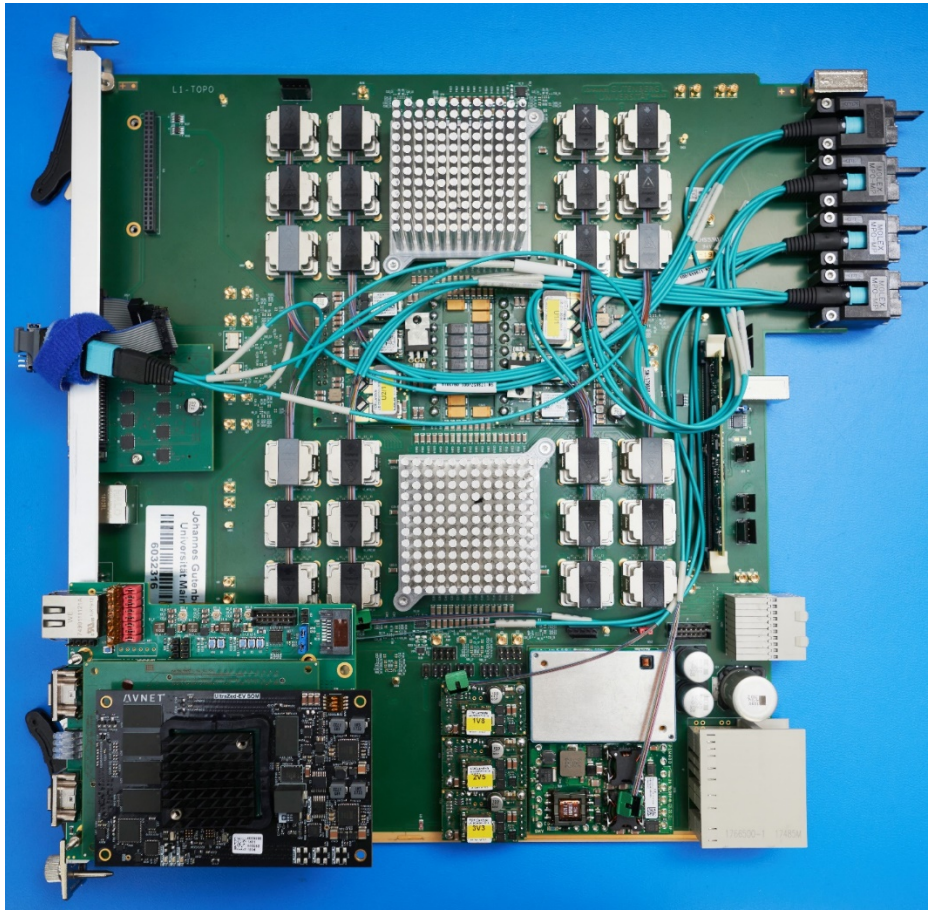
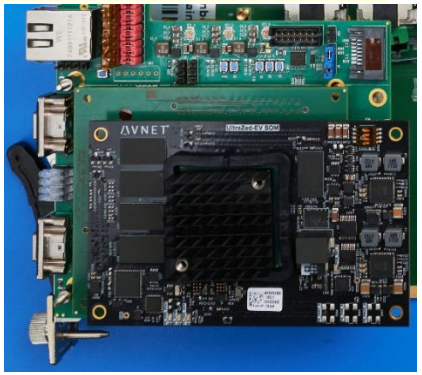


new

L1Topo 1st production module with control mezzanine v3.0

new

Control Mezzanine v3.0 General Functionalities



- Carrier board for the UltraZed-EV
- Functionalities
  - Hosts the control module of the **jFEX/L1Topo** mainboard
    - Zynq Ultrascale+ ZU7EV-FBV900
  - LHC clock cleaning and distribution to processor FPGAs
    - Si5345
  - Hosts the MasterSPI configuration circuitry for processors
    - MT25QU02GCBB8E12-0SIT
  - IPBus master
  - Hosts the PHY chip (transformer-less scheme)
    - VSC8221
  - TTC data reception and distribution to processor FPGAs
    - HUB1: Using fanout NB7VQ1006M
    - HUB2: Reception on one MGT and distribution to processors via IOs
  - Communication to mainboard CPLDs (PWR and CTRL_CLK)
  - Monitoring and slow control
    - MiniPODs (Avago) monitoring viaI2C
    - PMBus monitoring

Control Mezzanine v3.0 validation status

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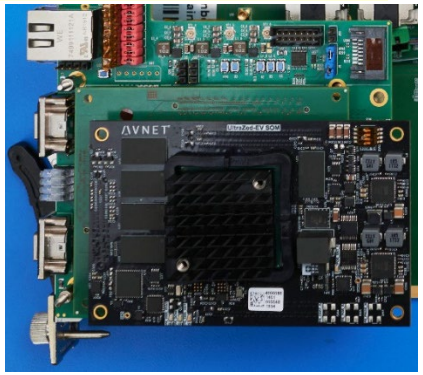


All functionalities have been fully validated on both jFEX and L1Topo! Ongoing production of final PCBs – total lead time, including assembly: 8 weeks

L1Topo Module tests / mainboard

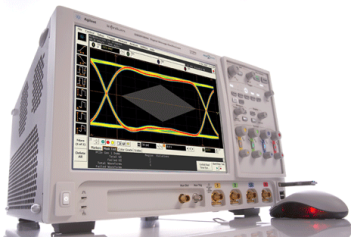
- The production module was stand-alone tested in the home lab
- Power consumption and ripple fully measured and reported
- Full Ibert tests of all interfaces at the STF
- Ipbus subsystem successfully tested (w. control mezzanine 3.0) at STF
- System-level tests at the STF successfully run
  - Formatted TOB data successfully received from the FEXes
  - Spy data BCReset sync'ed
  - L1Accept recorded along with real-time data
  - Stable data transmission
  - Trailer handling understood, final agreement required (see below)
- MUCTPI → L1Topo formatted data transmission tests yet to be done

Recently (double check on prototype → production fixes)

- Further link qualification tests: e/o MGT transmitter tests
- Keysight DSA91204 – 12 GHz bandwidth
  - Differential probe soldered on the miniPOD connector
  - Optical transceiver for direct fibre connection
- 12.8Gb/s PRBS-7 pattern chosen (→ reference for jFEX design update)

Last open issue wrt real-time data transmission:
Confirm TX link performance

Agilent/Keysight DSA91204



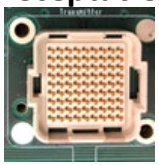
InfiniiMax II Amplifier

5425B Diff Probe Heads

N5426B ZIP Tip

(Soldered on a MiniPOD adapter)

MiniPOD Receptacle



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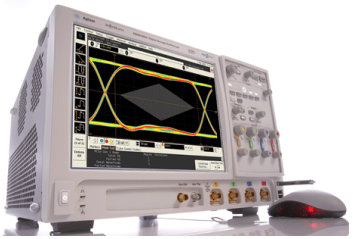
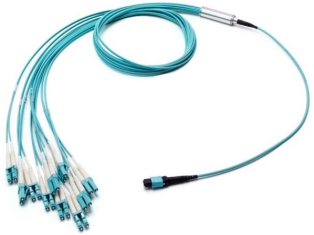


81495A Reference Receiver

LC to ST

MTP to LC



PRIZM to MTP

MiniPOD

Results – Channel X1Y21

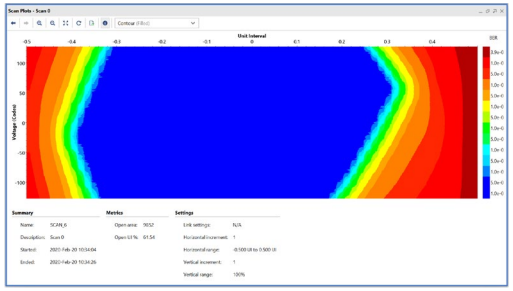
- A channel that had hadn’t been well understood in previous tests
- Tune the MGT parameters
- Make sure we are within MiniPOD specs (reduced swing)

Electrical; TX Setup 3; PRBS7

Eye opening within miniPOD mask specification

Optical; TX Setup 3; PRBS7

IBERT; TX Setup 3; PRBS7



Conclusions on link data integrity

- Very good eye opening for the L1Topo outputs, after properly setting the TX Pre-Emphasis parameters
  - Within the miniPOD specification
- Validation of the L1Topo Pre-Production module and the GTY calibration circuit
  - No significant difference wrt to Prototype

- → consider design fully validated

Firmware status

- Algorithms and input mapping has been reported on (Johannes) https://indico.cern.ch/event/884278/contributions/3745259/attachments/2004273/3346895/talk.pdf
- Real-time infrastructure (MGTs/SerDes) exists
  - Tested with FEXes at STF (protocol tests)
- Module control (Ipbus)
  - First version exists
    - Successfully operated with standalone software throughout STF tests
    - Recent improvement on play/spy module (BCR syc)
  - Being turned into a common framework L1Topo/jFEX
    - Online software for common scheme under way
- Along with control mezzanine v3.0 comes a set of f/w
  - I2C based monitoring of environmental data
- Readout firmware will be ported from jFEX soonish

→ Full integration yet to be accomplished:
real-time infrastructure / algorithms / control / readout

A few discussions on input TOB data formats…

- Had some initial issues with data formats from FEXes at early STF tests
- Mainly sorted out
- Some modifications to format specs still possible, not finally signed off
  - Discussion on optimal CRC scheme (Jira)
  - Request to add BCR bit to trailer of FEX TOBs
  - jFEX requested some of the "reserved" bits in trailer for overflow indication

→ Can be sorted out quickly → finalize input firmware soonish

L1Topo production status

- The production PCBs exist
- First module has been assembled, successfully been tested and reported on in this presentation
- Components available for remaining modules
- Expect assembly to take ~ 1 Month after green light from reviewers
- Production of a small batch of control mezzanines v.3.1 under way
  - No issues with PCB production expected
  - Assembly needs to be sorted out (previous batch assembled at CERN !)
- CTP interface module exists, ready for tests with CTP and volume production at any time

Summary / plans

- First L1Topo production board successfully tested
- Basically ready for production of remaining modules
- Firmware components in good shape
  - Algorithms see Johannes
  - Realtime infrastructure done and tested, minor fixes
  - Control firmware being restructured
  - Readout under way for jFEX (see Ren-Jie) → port to Topo
- Firmware integration time-consuming (multi-die FPGAs)
- Ready to install in USA15 in summer