Post PRR Status L1Topo

Uli / Mainz

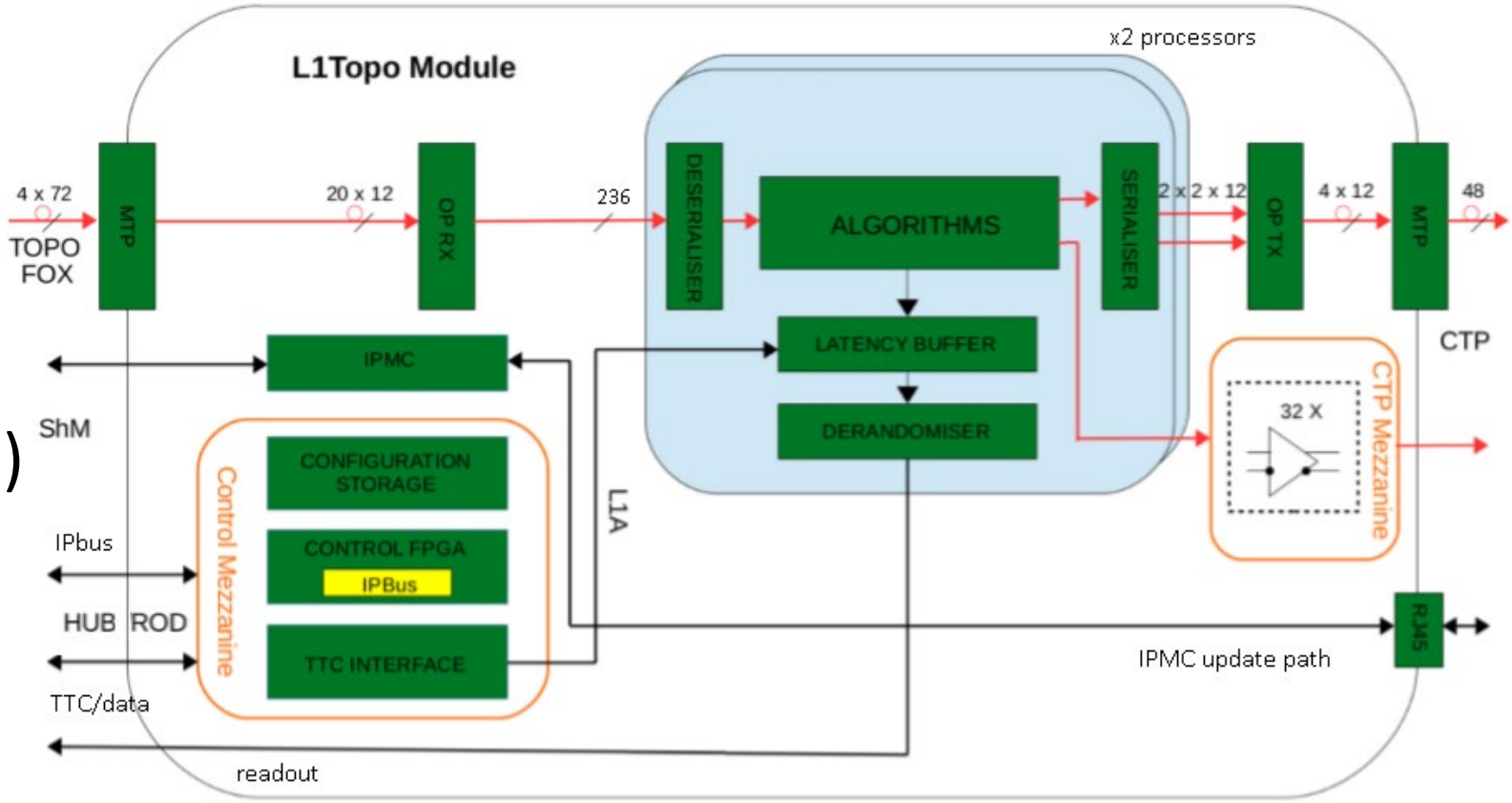
- Hardware overview
- Tests
- PRR Recommendations

Hardware Overview

- ATCA board (based on jFEX design)
- 2 Virtex UltrascalePlus

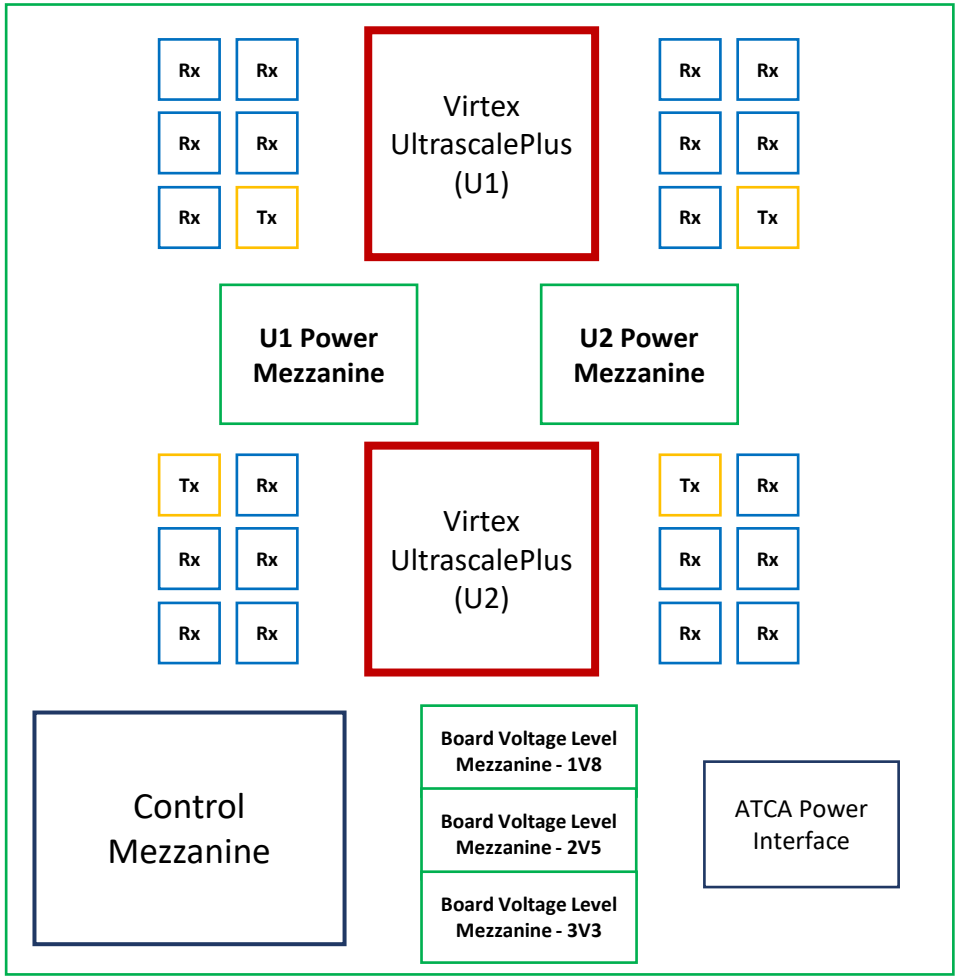
Two iterations

- Prototype (FDR 01/2019)
- Final design presented at PRR 08/2019



Hardware Overview

- ATCA board (based on jFEX design)
  - Modular design
- 2 Virtex UltrascalePlus FPGAs
  - XCVU9P-2FLGA2577E
  - 120 MGTs (GTY) per FPGA
    - 118 input fibres per processor FPGA
- 24 MiniPOD: 20 RX + 4 TX
- Mezzanines
  - Control & Power
  - Both compatible with jFEX



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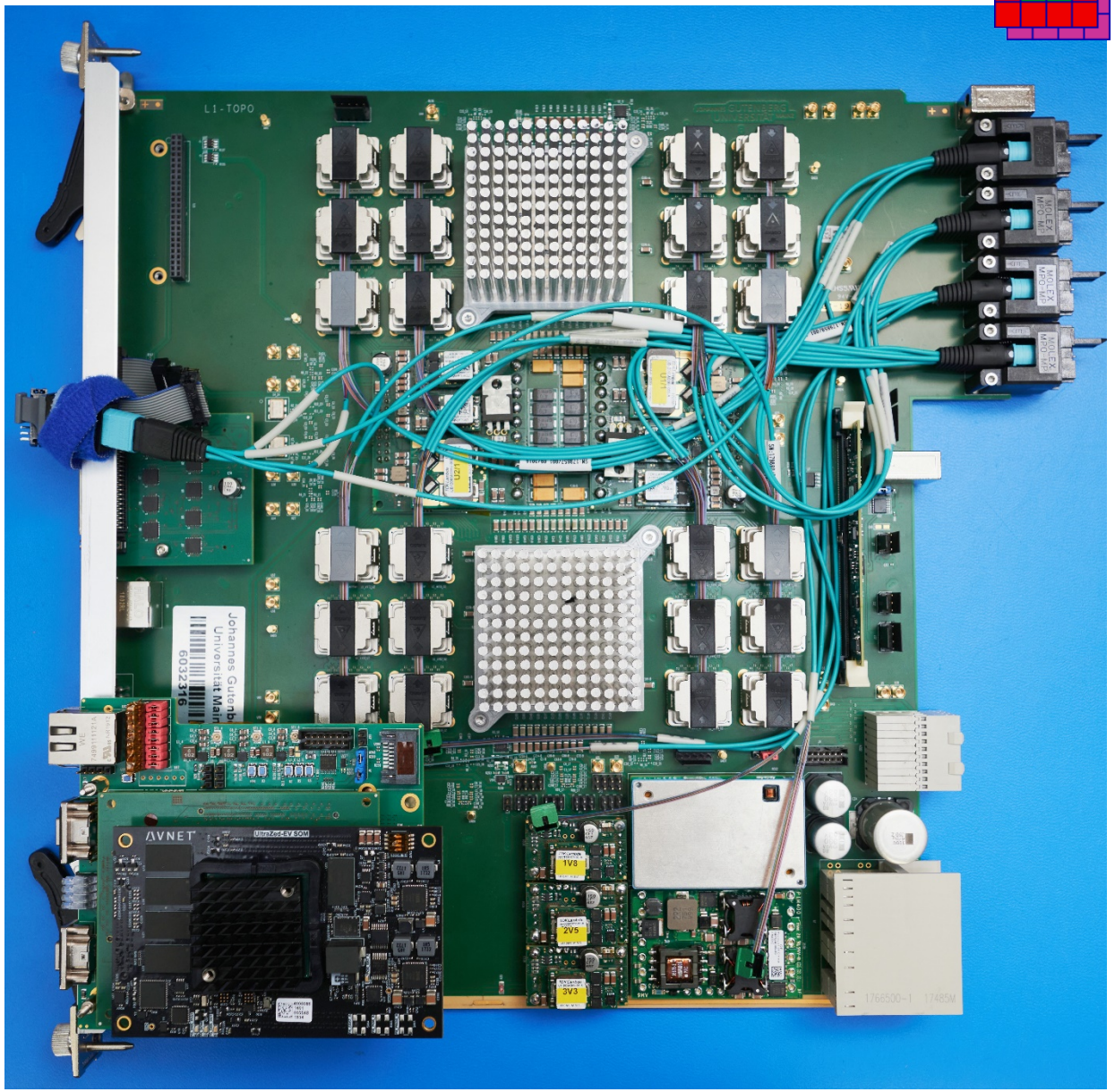
L1Topo 1st production module with “new” mezzanine



History: L1Topo **post-FDR** design modifications

Production vs. prototype, **presented at PRR** 08/2019

Mainboard-only

- **Correction of MGT termination calibration scheme**
- Correct a few items on the assembly list (resistor, capacitor values)
- Specify single ended clock lines to 50 Ω impedance
- Advise assembly company on backplane connector handling (solder vs press-fit)
- Add JTAG TCK fanout buffer to allow for proper 50 Ω series termination
- Correct Sysmon ADC pin VP/VN connection scheme / define unique I2C addresses for the two processor FPGAs
- Correct clock pair choice (non-) issue on MGT QUAD232

Mainboard-mezzanine interface (pinout to be consistent with the jFEX since the mezzanine is a common item)

- Correction of proper differential routing of spare lines between processor FPGAs and extension mezzanine
- Add module type coding on the mezzanine interface: selectively ground two as yet unused pins on connector
- Add further signal return GND connections to the mezzanine connector
- Connect Mainboard JTAG chain to mezzanine

Adapt IPM controller scheme to **CERN IPMC** and correct a few errors

- Correct and slightly extend USER_IO connectivity for purpose of IPMC / module controller data exchange
- Remove a few links that are unconnected on the CERN IPMC footprint
- Change JTAG header to Microsemi interface standard and connect reset line
- Remove spare connectivity for external, mezzanine based IPMC
- Move IPMC temperature sensors for better accessibility and functionality

History: control mezzanine

Functionality:

- Module controller (IPbus) with bridge to processor FPGAs
- Clock cleaning/synthesis and 1st stage of fanout
- Extended monitoring / I2C (-> IPbus)
- Configuration storage (SPI/SD)

Versions:

- Initially Zynq 7 based

→ UltraZed module, change of Ethernet Phy (device recommended for magnetics-free backplane operation)

- IPbus in PL
- Housekeeping / I2C in PS
- Currently Petalinux
- Looking into alternatives (some work done on kernel compilation and Debian & Centos rootfs)

Test, firmware, software status

- Module successfully tested with formatted input from all FEXes @ STF
- All real-time hardware interfaces successfully tested including CTP port
- Clocking, TTC data, and readout paths successfully tested
- Successful operation of IPbus, I2C subsystem, IPMC
- Algorithms status see Johannes
- V.1 Real-time infrastructure well tested
- V.1 Control firmware well tested
- Restructuring of firmware (V.2, common jFEX/Topo code) well advanced
- Integration with readout to be done as soon as readout firmware can be ported from jFEX code
- Online software (compatible to v.2 firmware) to be ported from jFEX asap

PRR recommendations, May 4, 2020

- The inter-FPGA parallel LVDS connectivity should be tested. Even though it has been stated there is currently no plan to use it, this may change.

→ to be done in Mainz soon

- A test of the interface between L1Topo and CTP should be carried out.

→ to be done at CERN asap

- The protocol test between MUCTPI and L1Topo should be performed.

→ to be done at CERN asap

- An optical attenuation test should be performed between gFEX and L1Topo in order to assess the optical power margin as for the other modules.

→ to be done at CERN asap

- The end-to-end link latency measurements should also be performed at the link speeds of 6.4 Gb/s and 11.2 Gb/s.

→ We are not assuming the MUCTPI to run at 6.4 Gb/s, but we will be able to do latency measurements along with MUCTPI tests

- The module power consumption and FPGA temperatures should be measured under realistic conditions using a complete, close to final, processing FPGA firmware.

→ Will be done once we have a fully integrated, final firmware

- The mapping of the TopoFOX fibers to the GT groups in the FPGAs should be checked at STF in order to make sure that the are no unexpected swaps.

→ Details to be discussed

- The assembled boards should go through a burn-in test with temperature cycles as stress screening.

→ Details to be discussed

PRR recommendations, continued…

- A few unfinished jobs, generally rather trivial and quickly done once we can make full use of the STF again
- The last two items on the list:
  - Input fibre mapping to quads: That comment was referring to some statement on bitrate mixing in quads we once made in an early version of our specifications which was actually referring to an initial pre-UltraScale+ design
  - The fibre mapping has been confirmed and understood to the extent possible at the STF
  - Final mapping tests will not be possible until installed at point 1
  - We do not want to show that there is no mixing, we want to show that mixed bitrate quads work properly without any concern
  - The assembled boards should go through a burn-in test with temperature cycles as stress screening.
  - My personal opinion: I am not going to destroy an expensive module in a burn-in procedure myself. A burn-in should be done only to an extent that the assembly company is ready to do and take responsibility for.

L1Calo: Risk of damaging one module unrecoverable during burn-in vs. possible infant death

Note: no money available to produce additional modules beyond nominal 3+2