

2013-03-05

Table 11: L1Topo

	ns	BCs	Sub Total	Total
Optical Input available from CMX, eFex, jFex & Muctpi				60.2
L1Topo Input Deserialisers	50	2.0		
Synchronize to local clock - 320-> 40 MHz	25	1.0		
Algorithmic Processing	125	5.0		
			8.0	
Electrical Output to CTP (multiplexed) (if used)	25	1.0		
Electrical Cable to CTP (if used) (2m)	10	0.4		
			1.4	
L1Topo electrical input available at CTP			69.6	L1Topo_Electrical
Output Multiplexers 40-320 MHz (if used)	25	1.0		
Output Serialisers for optics (if used)	50	2.0		
Fibres to CTP (if used) (2m)	10	0.4		
			3.4	
L1Topo Optical inputs to CTP available		11.4	71.6	L1Topo_Optical

Table 12: CTP

	ns	BCs	Sub Total	Total
Last Electrical Signal arrival				69.6
CTP Input Delay - Electrical Input		2.0		
CTP_In processing + PITbus		3.0		
Electrical input data ready in CORE		5.0	74.6	
Last Optical Signal Arrival			71.6	
Input deserialisers		2.0		
CTP Input Delay - Optical Input		2.0		
Optical input data ready in CORE		4.0	75.6	
Last Input Data available to CORE for processing			75.6	

Phase I    L1Topo and CTP Phase I    L1muon Phase I    Parameters    Summary    Contacts    UpdateLog    +

2020-08-05

Table 14: L1Topo

	ns	BCs	Sub Total	Total
Input available from CP_JE, eFex, jFex, gFex & Muctpi				64.3
L1Topo Input Deserialisers	50	2.0		
Synchronize to local clock - 320-> 40 MHz	25	1.0	3.0	
Algorithmic Processing	125	5		
Electrical Output to CTP (multiplexed) (if used)	25	1.0		
Electrical Cable to CTP (if used) (2m)	10.0	0.4	6.4	
L1Topo electrical input available at CTP			9.4	L1Topo_Electrical
Processing	100	4		
Output Multiplexers 40-320 MHz (if used)	25	1.0		
Output Serialisers for optics (if used)	50	2.0		
Fibres to CTP (if used) (2m)	10.0	0.4	7.4	
L1Topo Optical inputs to CTP available			10.4	L1Topo_Optical

Table 15: CTP

	ns	BCs	Sub Total	Total
Last CTP_IN Electrical Signal arrival				69.2
CTP_In processing + PITbus	49.9	2.0		
CTP_IN Electrical input data ready in CORE			2.0	71.2
Last Optical Signal Arrival			74.7	CTP_Direct_Optical
Input deserialisers	75	3.0		
Optical input data ready in CORE			3.0	77.7
Last CTP_CORE Direct Electrical Signal			73.7	CTP_Direct_Electrical
Signal Retiming	12.5	0.5		
CTP_CORE Electrical Input available to CORE			0.5	74.2
Last Input Data available to CORE for processing				77.7
New CTP_CORE: processing and output	149.7	6.0		
CTP Out				83.7

Table 6: iFEX

	ns	BCs	Sub Total	Total
Aug. 2020				47.5
Input data available - PPM, Tile opt I, LAr DPS				
Deserializer on jFex	50	2.0		
Data dupl between FPGAs via PMA Loopback	37	1.5		
Channel demultiplexing/synchronization	25	1.0		
Primitive processing (Jet, Energy Sums)	125	5.0		
Tob selection for output	25	1.0		
Multiplexing	25	1.0		
Serializer	50	2.0		
Optical cable (16.2m) to L1Topo via TopoFox		81	3.2	
Optical data available at L1Topo input	16.7	63.6	16.7	L1Calo_jFex

Table 6: iFEX

	ns	BCs	Sub Total	Total
Input data available - PPM, Tile opt I, LAr DPS			46.8	
Deserializer on jFex	50	2.0		
Data dupl between FPGAs via PMA Loopback	37	1.5		
Channel demultiplexing/synchronization	25	1.0		
Primitive processing (Jet, Energy Sums)	125	5.0		
Tob selection for output	25	1.0		
Multiplexing	25	1.0		
Serializer	50	2.0		
Optical cable (16.2m) to L1Topo via TopoFox		3.2		
Optical data available at L1Topo input	16.7	63.6	16.7	