Latencies jFEX / L1Topo

2020-09-04

jFEX - Aug 5 2020

Table 6: jFEX

Aug 20	ns	BCs	Sub Total	Total	
Input data available - PPM, Tile opt I, LAr DPS				47.5	
Deserializer on jFex	50	2.0			
Data dupl between FPGAs via PMA Loopback	37	1.5			
Channel demultiplexing/synchronization	25	1.0			
Primitive processing (Jet, Energy Sums)	125	5.0			
Tob selection for output	25	1.0			
Multiplexing	25	1.0			
Serializer	50	2.0	13.5		stable since 2015
Optical cable (16.2m) to L1Topo via TopoFox	81	3.2			add 1.2 in 2018
Optical data available at L1Topo input			**16.7**	64.3	

L1Topo

	2020-08-05					2013-05	
2	**Table 14: L1Topo**						
3		ns	BCs	Sub Total	Total		total
4	Input available from CP_JE, eFex, jFex, gFex & Muctpi				64.3		60.2
5	L1Topo Input Deserialisers	50	2.0			measured	
6	Synchronize to local clock - 320-> 40 MHz	25	1.0	**3.0**		estimated	
7							
8	Algorithmic Processing	125	5			estimated	
9	Electrical Output to CTP (multiplexed) (if used)	25	1.0			measured	
10	Electrical Cable to CTP (if used) (2m)	10.0	0.4	**6.4**		measured	
11	L1Topo electrical input available at CTP			9.4	73.7	L1Topo_Electrical	9.4 69.6
12	Processing	100	4			estimated	
13	Output Multiplexers 40-320 MHz (if used)	25	1.0			measured	
14	Output Serialisers for optics (if used)	50	2.0			measured	
15	Fibres to CTP (if used) (2m)	10.0	0.4	**7.4**		measured	
16	L1Topo Optical inputs to CTP available			**10.4**	74.7	L1Topo_Optical	11.4 71.6
17							
18	**Table 15: CTP**						
19		ns	BCs	Sub Total	Total		
20	Last CTP_IN Electrical Signal arrival				69.2	CTP_IN	
21	CTP_In processing + PITbus	49.9	2.0			measured	
22	CTP_IN Electrical input data ready in CORE			2.0	**71.2**	CTP_CORE_PIT	
23	Last Optical Signal Arrival				74.7	CTP_Direct_Optical	71.6
24	Input deserialisers	75	3.0			estimated	
25	Optical input data ready in CORE			3.0	**77.7**	CTP_Optical	**75.6**
26	Last CTP_CORE Direct Electrical Signal				73.7	CTP_Direct_Electrical	
27	Signal Retiming	12.5	0.5			estimated	
28	CTP_CORE Electrical input available to CORE			0.5	**74.2**	CTP_CORE_Electrical	
29	Last Input Data available to CORE for processing				77.7		
30	New CTP_CORE: processing and output	149.7	6.0			estimated	
31	CTP Out				83.7	CTP_L1A	
32							

Latencies – some thoughts

- jFEX latency hasn't changed for five years
  - Continuing to work on latency minimization (sub-ticks)
- L1Topo latency (electrical nor optical path) hadn't changed for more than 7 years
- Currently working on L1Topo latency reduction
  - optical path / multiplicities
  - Processing latency **down by one tick** in August 5 estimate
  - Let's be optimistic : get processing latency down a further few sub-ticks?

But:

- Any correlations between different object types difficult for results on the optical path !

Generally:

- Latencies cannot be determined by breaking down to individual contributions inside an FPGA, as they do not add up:
  t1, t2 → t1+t2+X
- Total latency is known once it has been measured in fully implemented firmware
- Neither infrastructure nor algorithms firmware 100% complete
- We are still fighting at the timing closure front
- Super logic region concept of large Xilinx FPGAs makes it more difficult than ever before → expect significant SLR crossing latency

Backup slides

jFEX, June 2015

edms.cern.ch/file/1256858/1/Working_Draft_Latency_Envelope_4Jun2015.xlsm

Table 6: jFEX June 4, 2015

	ns	BCs	Sub Total	Total	
Input data available - PPM, Tile opt I, LAr DPS				44.8	
Deserializer on jFex	50	2.0			
Data dupl between FPGAs via PMA Loopback	37	1.5			
Channel demultiplexing/synchronization	25	1.0			
Primitive processing (Jet, Energy Sums)	125	5.0			
Tob selection for output	25	1.0			
Multiplexing	25	1.0			
Serializer	50	2.0			
Optical cable (10m) to L1Topo	50	2.0			
Optical data available at L1Topo input			15.5	60.3	L1Calo_jFex

L1Topo, March 2013

edms.cern.ch/file/1256858/1/Working_Draft_Latency_Envelope_05Mar2013.xlsm

Table 11: L1Topo, Mar 05, 2013

	ns	BCs	Sub Total	Total	
Optical Input available from CMX, eFex, jFex & Muctpi				60.2	
L1Topo Input Deserialisers	50	2.0			
Synchronize to local clock - 320-> 40 MHz	25	1.0			
Algorithmic Processing	125	5.0			
			8.0		
Electrical Output to CTP (multiplexed) (if used)	25	1.0			
Electrical Cable to CTP (if used) (2m)	10	0.4			
			1.4		
L1Topo electrical input available at CTP				69.6	L1Topo_Electrical
Output Multiplexers 40-320 MHz (if used)	25	1.0			
Output Serialisers for optics (if used)	50	2.0			
Fibres to CTP (if used) (2m)	10	0.4			
			3.4		
L1Topo Optical inputs to CTP available			11.4	71.6	L1Topo_Optical

Table 12: CTP

	ns	BCs	Sub Total	Total	
Last Electrical Signal arrival				69.6	
CTP Input Delay - Electrical Input		2.0			
CTP_In processing + PITbus		3.0			
Electrical input data ready in CORE			5.0	74.6	
Last Optical Signal Arrival				71.6	
Input deserialisers		2.0			
CTP Input Delay - Optical Input		2.0			
Optical input data ready in CORE			4.0	75.6	
Last Input Data available to CORE for processing				75.6	
New CTP_CORE: processing and output		2.0			
CTP Out		2.5			
Cable to LTPi (10m)		2.0			
LTPi+LTP+TTCvi+TTCex		2.0			
Variable Delay		2.0			
			10.5	86.1	CTP_L1A