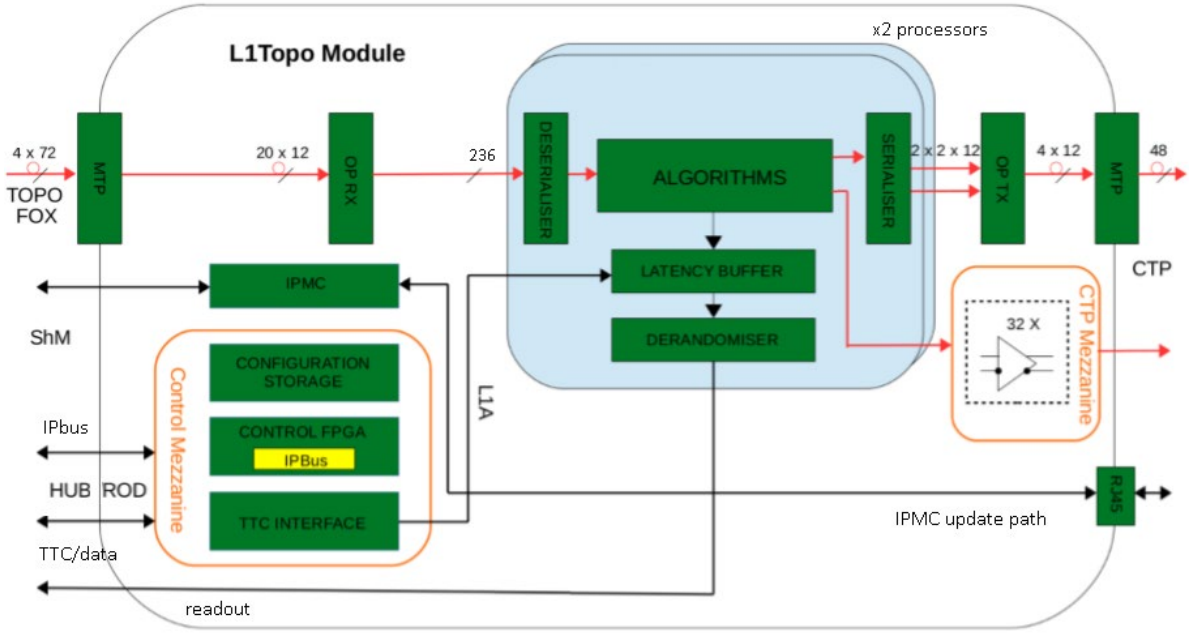
L1Topo status: hardware / tests / production / …

Uli / Mainz

Hardware Overview

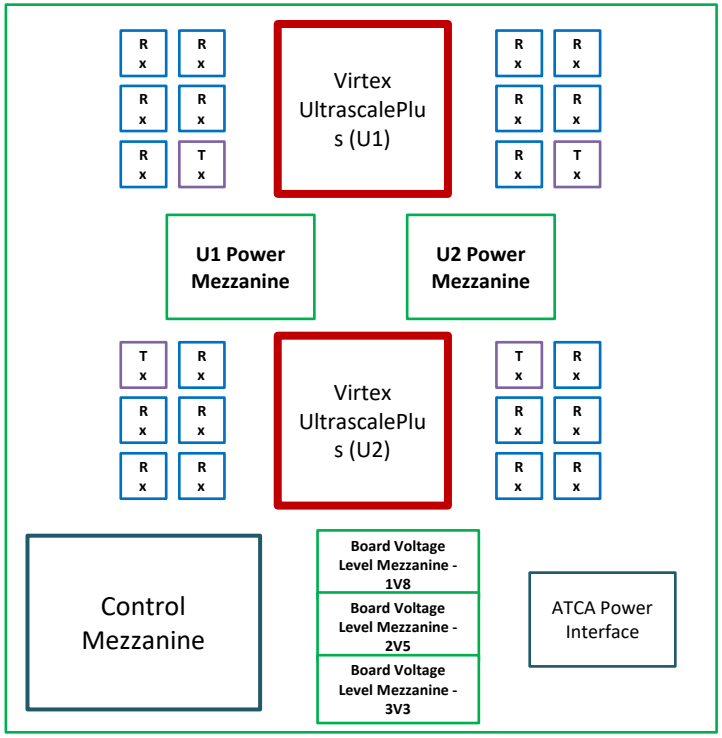
- ATCA board (based on jFEX design)
  - Modular design
- 2 Virtex UltrascalePlus FPGAs

- Two iterations
- Prototype (FDR 01/2019)
- Final design presented at PRR 08/2019
  - Fix on MGT calibration



Hardware Overview

- ATCA board (based on jFEX design)
  - Modular design
- 2 Virtex UltrascalePlus FPGAs
  - XCVU9P-2FLGA2577E
  - 120 MGTs (GTY) per FPGA
    - 118 input fibres per processor FPGA
- 24 MiniPOD: 20 RX + 4 TX
- Mezzanines
  - Control & Power
  - Compatible with jFEX
  - CTP interface module (LVDS drivers)



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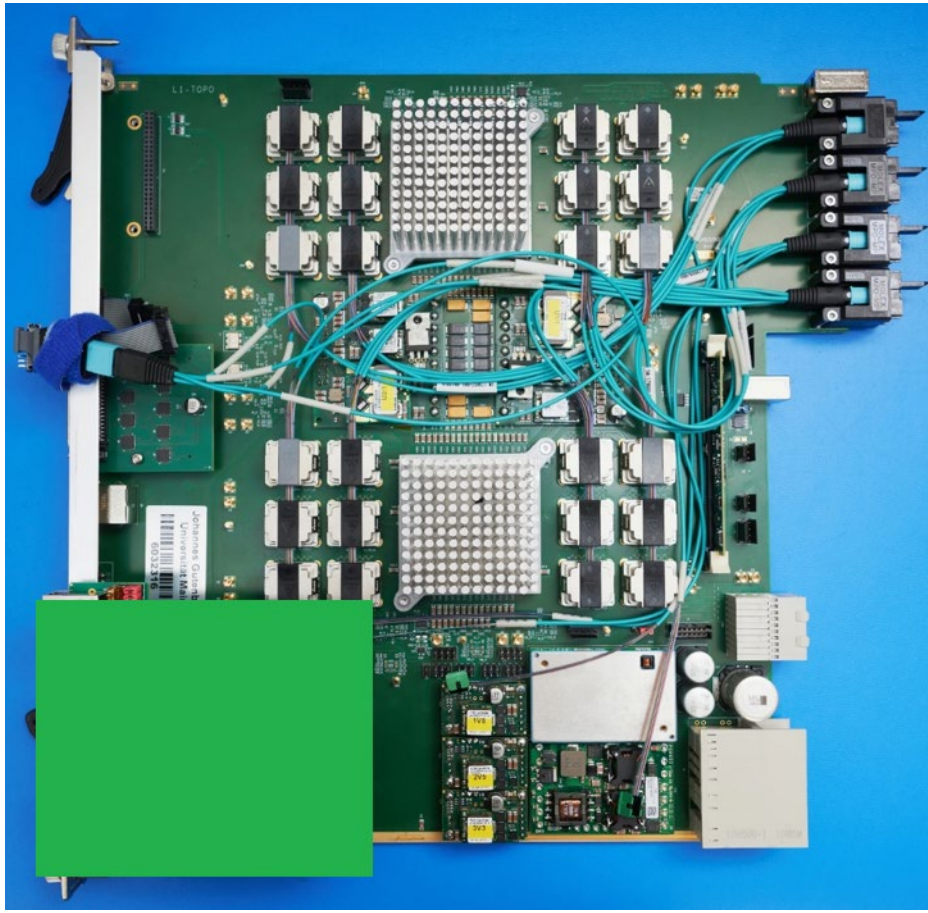
new

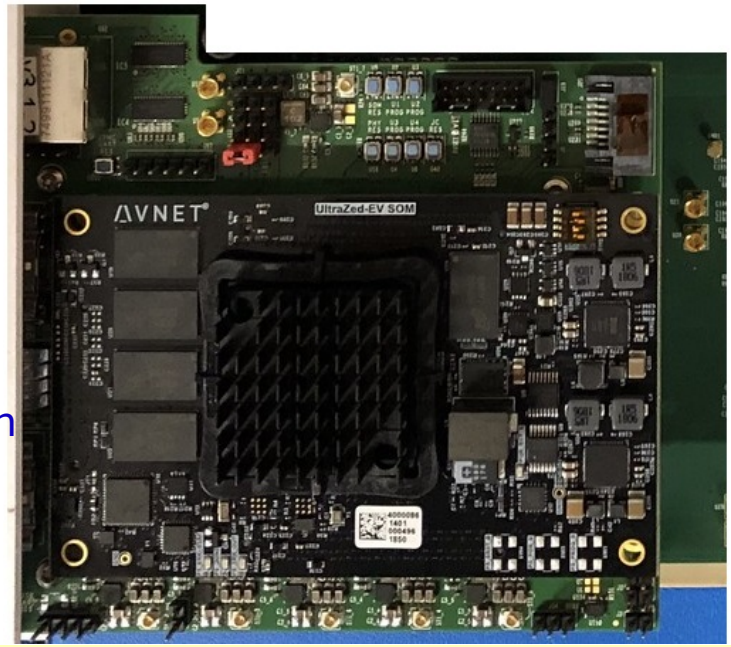
L1Topo 1st production module with control mezzanine v3.1



Control mezzanine v3.1

new

- Carrier board for UltraZed-EV SoM
  - Functionality equivalent to v3.0 shown in March TDAQ week, with minor fixes
  - **3** modules produced
  - Currently in use at STF on both **jFEX** and **L1Topo**
    - During last slice week
- Functionalities
  - Hosts the **control** module of the jFEX/L1Topo mainboard
    - **Zynq** Ultrascale+ ZU7EV-FBV900
  - LHC **clock** cleaning and distribution to processor FPGAs
    - Si5345
  - Hosts the MasterSPI **configuration** circuitry for processors
    - MT25QU02GCBB8E12-0SIT
    - **IPBus** master
      - Port selection between backplane or front-panel RJ45 with ETH MUX
  - Hosts the PHY chip (transformerless scheme)
    - VSC8221
  - **TTC data** reception and distribution to processor FPGAs
    - HUB1: Using fanout NB7VQ1006M
    - HUB2: Reception on one MGT and distribution to processors via parallel I/Os
  - **Monitoring** and slow control
    - MiniPODs (Avago) monitoring via **I2C**
    - PMBus monitoring



Controller test status

- Smoke tests, power sequencing
- Ripple measurement (MGT)
- Power up with UltraZed connected
  - Re-check **ripple** for MGT power rails
- JTAG access to Zynq
- **Booting** and configuring from SD card
- Ethernet MUX
  - Zynq PL (**IPBus**)
    - Backplane / front RJ45
  - Zynq PS
- I2C access to Si5345 (**jitter** cleaner)
  - Monitor status of inputs and outputs
- Reception of TTC **clock** via backplane with Si5345
- Check clock reception at FPGA from Si5345
- SPI **configuration** of processor FPGAs
- TTC combined data reception from **Hub slot 1**

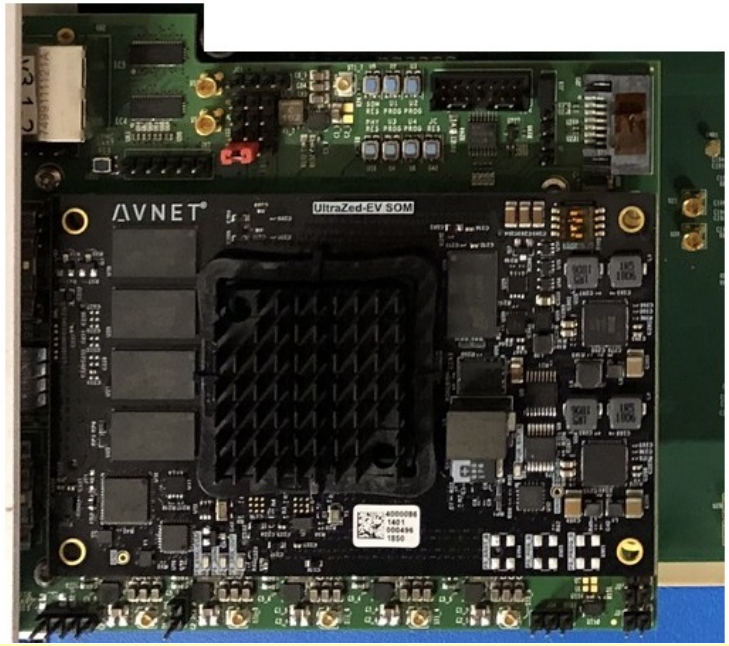
All **3** modules tested:

Done ✓

To be done

- **Monitoring** and slow control of Si5345 and mainboards MiniPODs, DC/DC converters
- Reception of TTC combined data from **Hub slot 2** and distribution to processors via I/Os
- Slot dependent IP/MAC
- IPBus stress test

→ **Production**



Mainboard test status

One prototype, one production module so far, minor differences

- Both generations of modules thoroughly tested in home lab and at the STF (standalone and slice)
- Modules successfully tested with formatted input from all FEXes @ STF
- Data reception confirmed by (BC sync'ed) spy mem readout
- Specific optical attenuation tests done, the last missing one (reviewers' request) quite recently
- All real-time hardware interfaces successfully tested in-depth, including CTP port
- Clocking, TTC data, and readout paths successfully tested
- Successful operation of IPbus, I2C subsystem, IPMC

- Some interfaces tested standalone / IBERT / electrical/optical only
- System tests done with **non-final firmware**

Further steps

Need to make progress on firmware completion

- Due to menu dependency, algorithms will never be “final”, just frozen.
- Finalize infrastructure firmware (common code base with jFEX)
- Adapt readout firmware (common code)
- **Integrate** infrastructure, readout, frozen algorithms (**timing closure**)

Then

- Repeat slice tests
- Confirm **latency** at system and link level

Some specific tests as requested in the PRR report May 4, 2020

- Interface test L1Topo / CTP
- **Protocol** test between MUCTPI / L1Topo
- Power consumption and FPGA temperatures under full firmware load
- Inter-FPGA parallel LVDS connectivity verification.

And yet further…

Once tests are finished…

"Volume production", for a total of 5 modules

- PCBs available
- Components available
- Should take ~6 weeks

- Completing the modules in the home lab and testing should happen at less than a week per module

Installation

- Installation is what happens before the modules slide in…
- Rack situation still unclear (?)
- Don't expect any commuters to go out to CERN any time soon

→ Limited effort available at CERN, needs careful planning

Summary

- L1Topo and its mezzanines well and tested
- Ready to go into production as soon as:
  - A few PRR recommended tests done
  - Firmware considerably improved and completed
  - Final tests at STF done
    … including final (*) latency figures
- Perhaps some open questions about installation at P1

(*) final = determined for a snapshot of algorithms integrated with high-speed infrastructure, control, and readout