

fFEX input data

Some initial discussions last year (Arno)

- Link speed 25(.65065/.78125 ?) Gbps
- 64/67bit encoding
- Link count : 3 options as of Oct. 16, 2019. Favourite option 2 „2) 0.1 x 0.1 E-Sums for $2.2 < \eta < 2.5$ separate per layer in EMEC and HEC; and all cells from $\eta > 2.5$: 492 fibres“
- Includes 100% duplication at source
 - Required for mapping sliding window type algorithms to a set of FPGA processors
 - Map a core plus an environment shared with neighbour onto given processor
 - Allows for getting full $\eta \times \pi/2$ core into a processor (phi quadrant)
 - With an environment of $\pm \pi/4$
 - Each processor covering full η range per detector side

>> confirm link parameters and define data mapping <<
see below

fFEX Module

- Minimum η, ϕ coverage per FPGA defined by required environment in jet algorithm, and data duplication at source
 - Large numbers of high speed links per FPGA
 - → large number of opto link devices
 - Reasonable partitioning into modules
 - **Two FPGAs** per module (ϕ quadrant each)
 - Two modules covering each detector end
 - **Four modules** in full fFEX system
 - ATCA based
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- ... let's have a look →

fFEX... looking a bit like L1Topo

But just a bit:

MiniPOD → Firefly

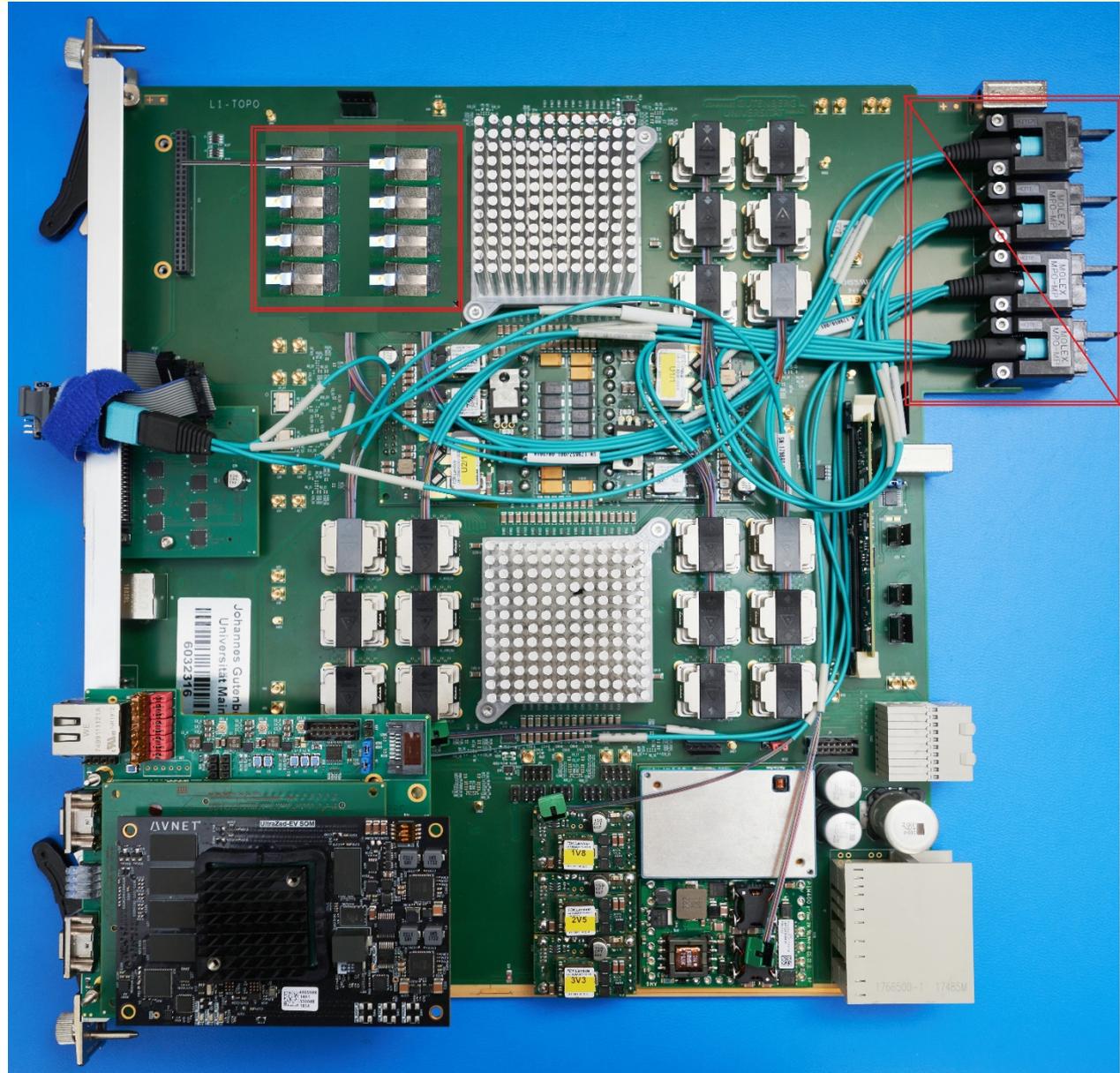
No solution for fibre aggregation from FireFly

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MTP-CPI → front MTP

R/O, timing → FELIX

Module controller TBD

Real-time output TBD



Urgent: Input link specification

- Upstream duplication: each data link sent twice
- Link speed to be confirmed
- Encoding to be confirmed
- (Calo data granularity to be agreed on) →
- Data volume to be confirmed
- Data format to be defined
 - Payload
 - bit count per channel
 - Can we gain from higher resolution?
 - Non? Linear? Encoding
 - Channel count per link
 - Channel mapping
 - Trailer
- Choice of FPGA/MGT type should be transparent: Xilinx, Intel
- Choice of opto link type should be transparent, but should probably be discussed: baseline FireFly