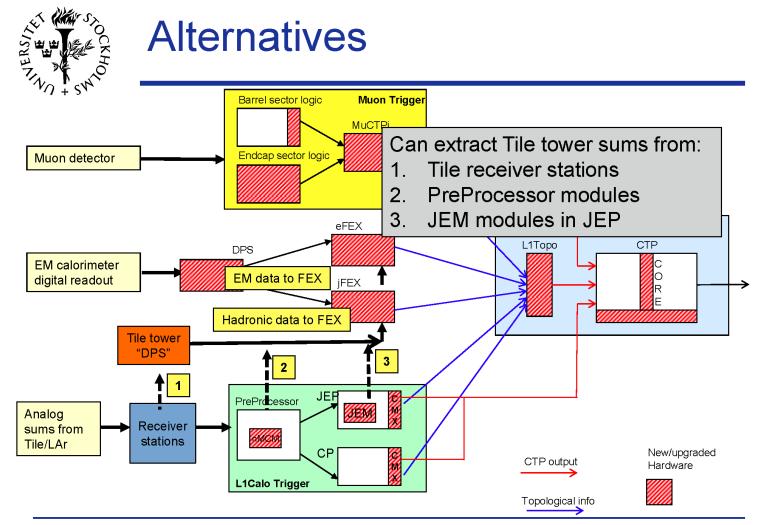
Latency / Tilecal o/e converters VME extender

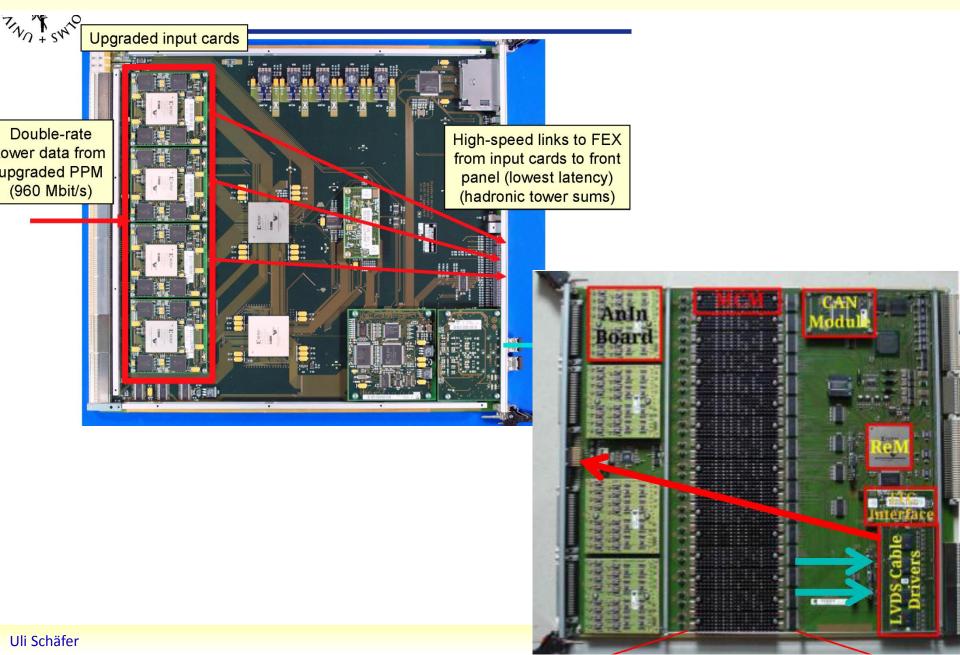
Tilecal o/e converters

 https://indico.cern.ch/getFile.py/access?contribId=101&s essionId=8&resId=1&materialId=slides&confId=158040



3

The two L1Calo based options (2, 3)





Option 2: PreProcessor

- Minimal latency:
 - Essentially equal to option 1;
- Can extend dynamic range:
 - nMCM can drive outputs at higher rates, so more bits per tower possible
 - 'Easy' to get 9 bits, 10 bits probably possible
- Relatively low cost
 - nMCM will already exist
 - A few (small) LVDS link boards
 - Possibly need to replace some PreProcessor mother boards (8 layers, low component count)
- Low disruption: Only upgrading existing boards

Option 3: JEM upgrade

- Higher latency:
 - Serial transmission from PPr to JEP adds multiple BCs to latency
- Limited dynamic range:
 - BCMUX protocol consumes some bandwidth
 - 9 bits possible (by removing parity), 10 bits probably not possible
- Similar cost to Option 2
 - PreProcessor nMCM and link cards still get replaced (but not PPr mother boards?)
 - Plans to upgrade JEM daughter boards anyway
- Low disruption: Again, similar to Option 2



Option 2 favored over 3

- Lower latency
- Fewer boards in the hardware chain
 - Everything on the PreProcessor
- Easier to expand/change dynamic range
- When would we use option 3?
 - Only if we can't get optical data out of the PreProcessor directly.
 - Options being considered...no show-stoppers seen yet

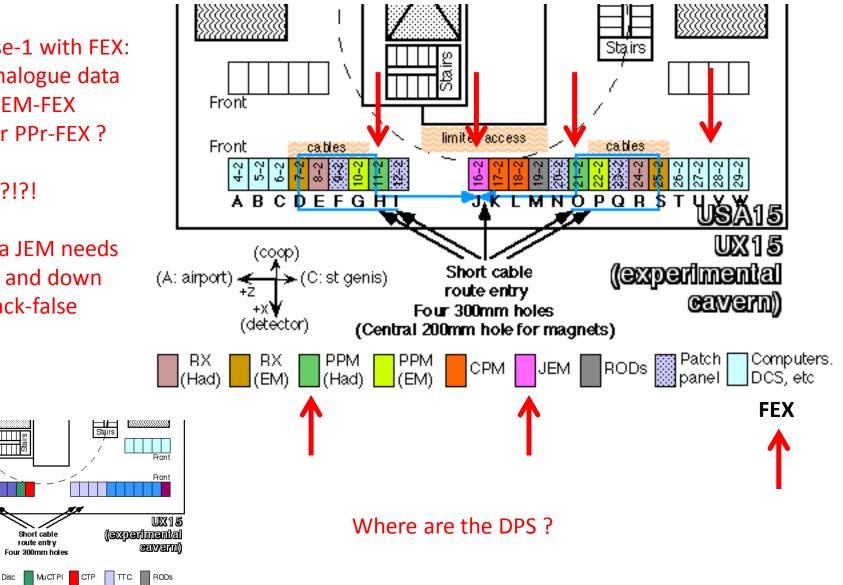
9

Cable/fibre routing USA15

For phase-1 with FEX: Route analogue data via PPr-JEM-FEX Or rather PPr-FEX ?

Latency ?!?!

Route via JEM needs to go up and down twice (rack-false floor)



(A: airport) - (C: st genis)

Muons (BPC)

Front

Latencies (from "Report of the ATLAS Calorimeter & Trigger Working Group")

		BČs	Sub Total	Total	
	LAR Analog (TTB+Receivers)				LAR Analog + Digital (LTD
	Time-of-flight to endcap at eta = 2	0.6			Time-of-flight to endcap at eta = 2
	Cable to pulse preamplifier	1.2			Cable to pulse preamplifier
	Pulse preamplifier and shaper	0.4	2.2	2.2	Pulse preamplifier and shaper
	Pulse peaking time	2	2.2	2.2	Pulse peaking time
	Cable to tower-summation board	0.2			Digitization on LTDB
	Analog summation	0.4			Multiplexing on LTDB
	Cable to USA15 (70 m)	14			Serializer on LTDB
	Receiver station				Optical cable (70 m) from LTDB to DPS
	Cable via patch panel and PPM	3.4			
			20	22.2	Deserializer on DPS
					Channel demultiplexing on DPS
	L1Processors				Channel demultiplexing on DPS Pedestal subtraction
	L1Processors				
					Pedestal subtraction
	PPM (preprocessor for e/gamma, tau/hadror	14			Pedestal subtraction
	PPM (preprocessor for e/gamma, tau/hadror LVDS Cable to CPM (11m)	2.2			Pedestal subtraction E, t. Q, N-tap FIR, BCID Digitial summation
	PPM (preprocessor for e/gamma, tau/hadror LVDS Cable to CPM (11m) CPM (cluster processor module)	2.2 13.5			Pedestal subtraction
	PPM (preprocessor for e/gamma, tau/hadror LVDS Cable to CPM (11m)	2.2	37.7		Pedestal subtraction E. t. Q. N-tap FiR, BCID Digitial summation Multipexing on DPS
tfinding	PPM (preprocessor for e/gamma, tau/hadror LVDS Cable to CPM (11m) CPM (cluster processor module)	2.2 13.5	37.7		Pedestal subtraction E. t. Q. N-tap FiR, BCID Digitial summation Multiplexing on DPS Senalizer on DPS
t finding arallel w.	PPM (preprocessor for e/gamma, tau/hadror LVDS Cable to CPM (11m) CPM (duster processor module) CMX (updated CP CMM, excluding serializers	2.2 13.5 8	37 <i>.7</i>		Pedestal subtraction E. t. Q. N-tap FiR, BCID Digitial summation Multiplexing on DPS Senalizer on DPS
t finding rallel w.	PPM (preprocessor for e/gamma, tau/hadror LVDS Cable to CPM (11m) CPM (duster processor module) CMX (updated CP CMM, excluding serializers PPM (preprocessor for jet, Et)	2.2 13.5 8 15.5	37.7		Pedestal subtraction E. t. Q. N-tap FiR, BCID Digitial summation Multiplexing on DPS Senalizer on DPS
tfinding arallel w.	PPM (preprocessor for e/gamma, tau/hadror UDS Cable to CPM (11m) CPM (dutater processor module) CMX (updated CP CMM, excluding senializers PPM (preprocessor for jet, Et) UVDS Cable to JEMS (11m)	2.2 13.5 8 15.5 2.2	37.7		Pedestal subtraction E, t, Q, N-tap FIR, BCID Digitial summation Multipleange on DPS Senalizer on DPS Optical cable (15 m) from DPS to FEX
t finding arallel w.	PPM (preprocessor for e/gamma, tau/hadror LVDS Cable to CPM (11m) CPM (duster processor module) CMX (updated CP CMM, eccluding senalizers PPM (preprocessor for pLE, Et) LVDS Cable to JEMs (11m) JEM (jet Et processor module)	2.2 13.5 8 15.5 2.2 7.5 9	37.7 34.2	59.9	Pedestal subtraction E, t, Q, N-tap FIR, BCID Digitial summation Multiplexing on DPS Serializer on DPS Optical cable (15 m) from DPS to FEX FEX Descrializer on FEX Data duplication between FPGAs
Et finding arallel w.	PPM (preprocessor for e/gamma, tau/hadror LVDS Cable to CPM (11m) CPM (duster processor module) CMX (updated CP CMM, eccluding senalizers PPM (preprocessor for pLE, Et) LVDS Cable to JEMs (11m) JEM (jet Et processor module)	2.2 13.5 8 15.5 2.2 7.5 9 2.2		59.9	Pedestal subtraction E, t, Q, N-tap FIR, BCID Digital summation Multiplexing on DPS Senalizer on DPS Optical cable (15 m) from DPS to FEX FEX Descrializer on FEX Data duplication between FPGAs Channel demultiplexing/synchronizatio
finding allel w.	PPM (preprocessor for e/gamma, tau/hadror UVD Scable to CPM (11m) CPM (duster processor module) CMX (updated CP CMM, excluding serializers PPM (preprocessor for jet, Et) UVD Scable to EMS (11m) IEM (get Et processor module) CMX (updated //E CMM, excluding serializers Cable to CTP (11m) for trigger sums CAMS Uchurk Serializers	2.2 13.5 8 15.5 2.2 7.5 9 2.2 2		59.9	Pedestal subtraction E, t, Q, N-tap FIR, BCID Digitial summation Multiplexing on DPS Sensilizer on DPS Optical cable (15 m) from DPS to FEX Desensilizer on FEX Data duplication between FPGAs Channel demultiplexing/synchronizabo Prinsibve processing (Agramms, KuA)
	PPM (preprocessor for e/gamma, tau/hadror LVD5 Cable to CPM (11m) CPM (duster processor module) CMX (updated CP CMM, excluding serializers PPM (preprocessor for iet, Et) LVD5 Cable to IEMs (11m) IEM (get Et processor module) CMX (updated I/E CMM, excluding serializers Cable to CTP (11m) for trigger sums	2.2 13.5 8 15.5 2.2 7.5 9 2.2		59.9	Pedestal subtraction E, t. Q, N-tap FIR, BCID Digitial summation Multiplexing on DPS Senalizer on DPS Optical cable (15 m) from DPS to FEX FEX Descrializer on FEX

LAR System Upgrade Scenario 1 (L1 only)

Sub Total

Total

	603	300 Iotal	Iotai
LAR Analog + Digital (LTDB+DPS)			
Time-of-flight to endcap at eta = 2	0.6		
Cable to pulse preamplifier	1.2		
Pulse preamplifier and shaper	0.4	2.2	
Pulse peaking time	Ο	2.2	2.2
Digitization on LTDB	7		
Multiplexing on LTDB	1		
Serializer on LTDB	2		
Optical cable (70 m) from LTDB to DPS	14		
		24	26.Z
Deserializer on DPS	2		
Channel demultiplexing on DPS	1		
Pedestal subtraction	1		
E, t, Q, N-tap FIR, BCID	5		
Digitial summation	2		
Multiplexing on DPS	1		
Serializer on DPS	2		
Optical cable (15 m) from DPS to FEX	3		
	-	17	43.2
FEX			
Deserializer on FEX	2		45.Z
Data duplication between FPGAs	0.5		45.7
Channel demultiplexing/synchronization	1		46.7
Primitive processing (e/gamma, tau/hadron, jet, E	5		51.7
Multiplexing	1		52.7
Serializer	2		54.7

2

What is the latency of the PPr / JEM path wrt the Lar DPS path ?

42

	BCs Sub Total		Total	
L1Topo				
1Topo Input Deserializers	Z			
Synchronize to local clock	0.5			
Algorithmic Processing	1			
		3.5		
Electrical Output to CTP	0.5			
Eectrical Cable to CTP (2m)	0.4			
		0.9		
Dutput Serializers for optics (if used)	2			
Fibrest to CTP (if used) (2m)	0.4			
		2.4		
		5.9	70	

CTP Input Delay		2.5	72.6
Last Electrical Signal arrival			
CTP_In processing + PITbus	3		
Last Input Data available for processing			
New CTP_CORE: processing and output	z		
CTP Out	2.5		
Cable to LTPi (10m)	2		
LTPi+LTP+TTOvi+TTCex	z		
Variable Delay	2		
		13.5	85.1
Fibers to FE electronics (110m)	22		
TTCReceiver	4		
		25	112.1
TOTAL			112.1

Figure 13.3. Detailed estimates of the L1 latency budget in Phase-I

latencies

LAr + L1Calo

	BĊs	Sub Total	Tota
LAR Analog (TTB+Receivers)			
Time-of-flight to endcap at eta = 2	0.6		
Cable to pulse preamplifier	1.2		
Pulse preamplifier and shaper	0.4		
		2.2	2.
Pulse peaking time	2		
Cable to tower-summation board	0.2		
Analog summation	0.4		
Cable to USA15 (70 m)	14		
Receiver station			
Cable via patch panel and PPM	3.4		
		20	22.

in parallel w. jet/Et finding	PPM (preprocessor for e/gamma, tau/hadror LVD5 Cable to CPM (11m)	14 - 2.2	→ ???	
	CPM (cluster processor module)	13.5		
	CMX (updated CP CMM, excluding serializers	8	- +3	
			37.7	
in parallel w.	PPM (preprocessor for jet, Et)	15.5		
e/g, t/h	LVDS Cable to JEMs (11m)	2.2		
	JEM (jet Et processor module)	7.5		
	CMX (updated J/E CMM, excluding serializers	9		
			^{34.2} _ 2	59.9
	Cable to CTP (11m) for trigger sums	2.2	т5	
	CMX Output Serializers	2		
	Optical Fibers to L1Topo (11m)	2.2		
			4.2	64.1

LAR System Upgrade Scenario 1 (L1 only)

	BCs	Sub Total	Total
LAR Analog + Digital (LTDB+DPS)			
Time-of-flight to endcap at eta = 2	0.6		
Cable to pulse preamplifier	1.2		
Pulse preamplifier and shaper	0.4		
		2.2	2.2
Pulse peaking time	0		
Digitization on LTDB	7		
Multiplexing on LTDB	1		
Serializer on LTDB	2		
Optical cable (70 m) from LTDB to DPS	14		
		24	26.2
Deserializer on DPS	2		
Channel demultiplexing on DPS	1		
Pedestal subtraction	1		
E, t, Q, N-tap FIR, BCID	5		
Digitial summation	2		
Multiplexing on DPS	1		
Serializer on DPS	2		
Optical <u>cable (15 m)</u> from DPS to FEX	<u>3</u>	17	43.2
41.4 + opt cable			
FEX			
Deserializer on FEX	2		45.2
Data duplication between FPGAs	0.5		45.7
Channel demultiplexing/synchronization	1		46.7
Primitive processing (e/gamma, tau/hadron, jet, E	5		51.7
Multiplexing	1		52.7
Serializer	2		54.7

z

Optical cable (10m) to L1Topo

56.7

56.7

13.5

Latency

- 3 ticks have been assumed for the e/o conversion including serialisation
- Depends on exact data format on incoming electrical stream.
- Larger, if de-serialisation to 40 Mb/s required
- Slightly smaller if data can be packed into 320Mb/s words on-the-fly
- Possibly even smaller if going to more than the baseline rate of 6.4Gb/s
- Optical cable length probably 3 ticks.
- PPM nMCM specs talking about 16 ticks for MCM and nMCM ! (previous slide: 14 / 15.5)
- Where are the DPS ? Is their 15m fibre length realistic ?
- F. Lanni: assumes that DPS path has higher latency than PPr path

VME extender/serialiser

- GOLD (and early L1Topo) module control via a chain 9U-crate CPU \rightarrow BLT \rightarrow GOLD (fibre, 1-2Gb/s) (Andreas)
- Long term replacement by Ethernet control (2014 ?)
 → IPBus workshop next week (Bristol) (or Zynq based scheme)
- Need medium term solution, since 9U/BLT approach not viable at CERN (early system tests)
- Build 6U VME extender
 - 6U VME module
 - Daughter module concept ?
 - Almost passive 6U mainboard ~4 layers, carrying level translators, possibly a CPLD (XC95?), ~4 SFPs ?, FPGA module
 - Enclustra Mars AX3 ?
 - SO-DIMM form factor seems suitable
 - VME slot width ~20mm
 - Not sure about availability of MGT links
 - Documentation seems outdated since it refers to XC7A30T which has been withdrawn by Xilinx
 - Let's try and design for the AX3 pinout, if we can get hold of it. If Enclustra aren't able to deliver, we will build our own module (production silicon available from Jan.2013 ?
 - Reinhold (h/w) + NN (A.R. ? h/w, f/w)....

 \rightarrow start now !

Other...

http://www.mcc-us.com/iportfaq.htm

 IPORT : Tools to control I2C from a PC (for lab / debug purposes)

- Other people are already working on microPOD
- Evaluation board
- Test board BNL



