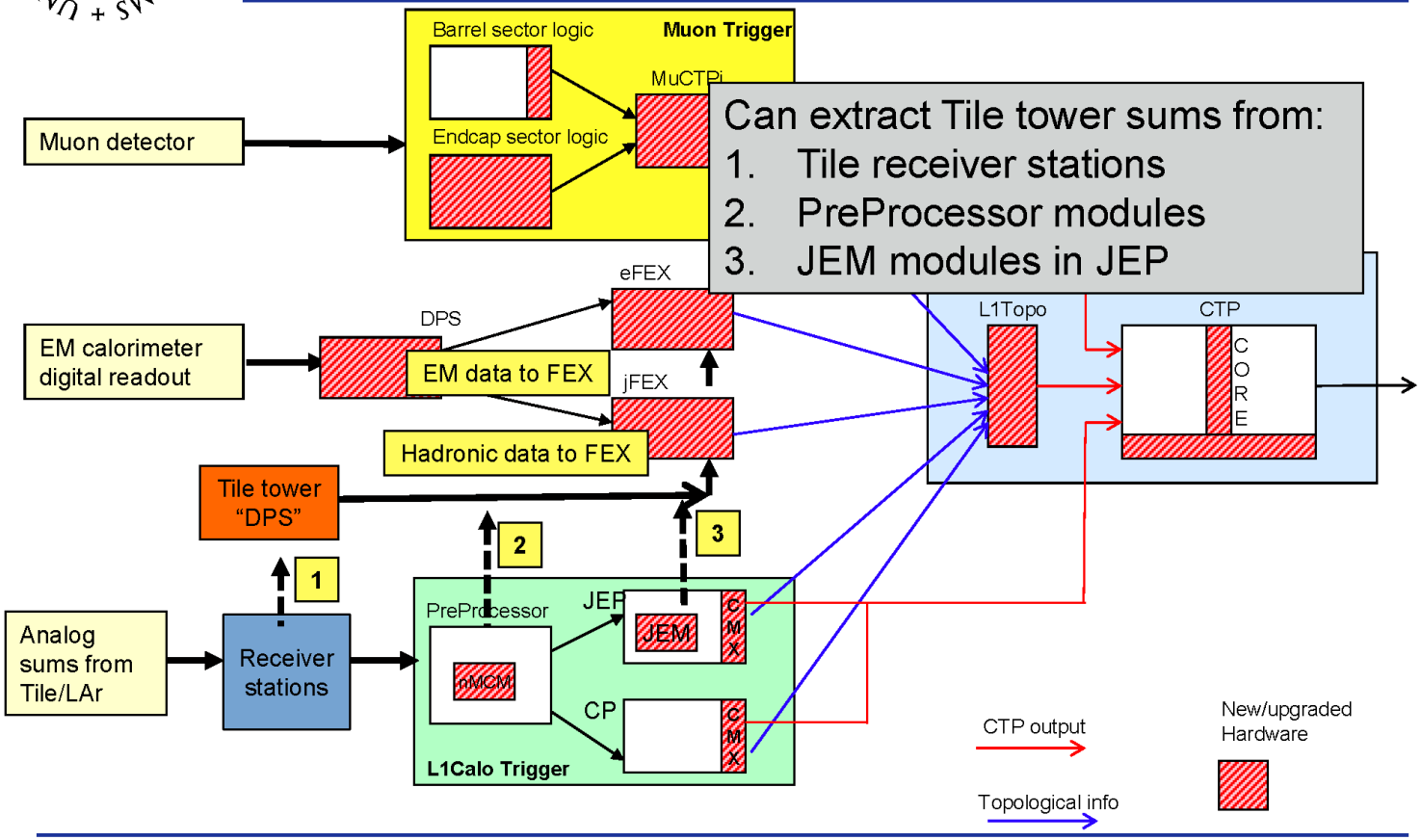
Latency / Tilecal o/e converters

VME extender

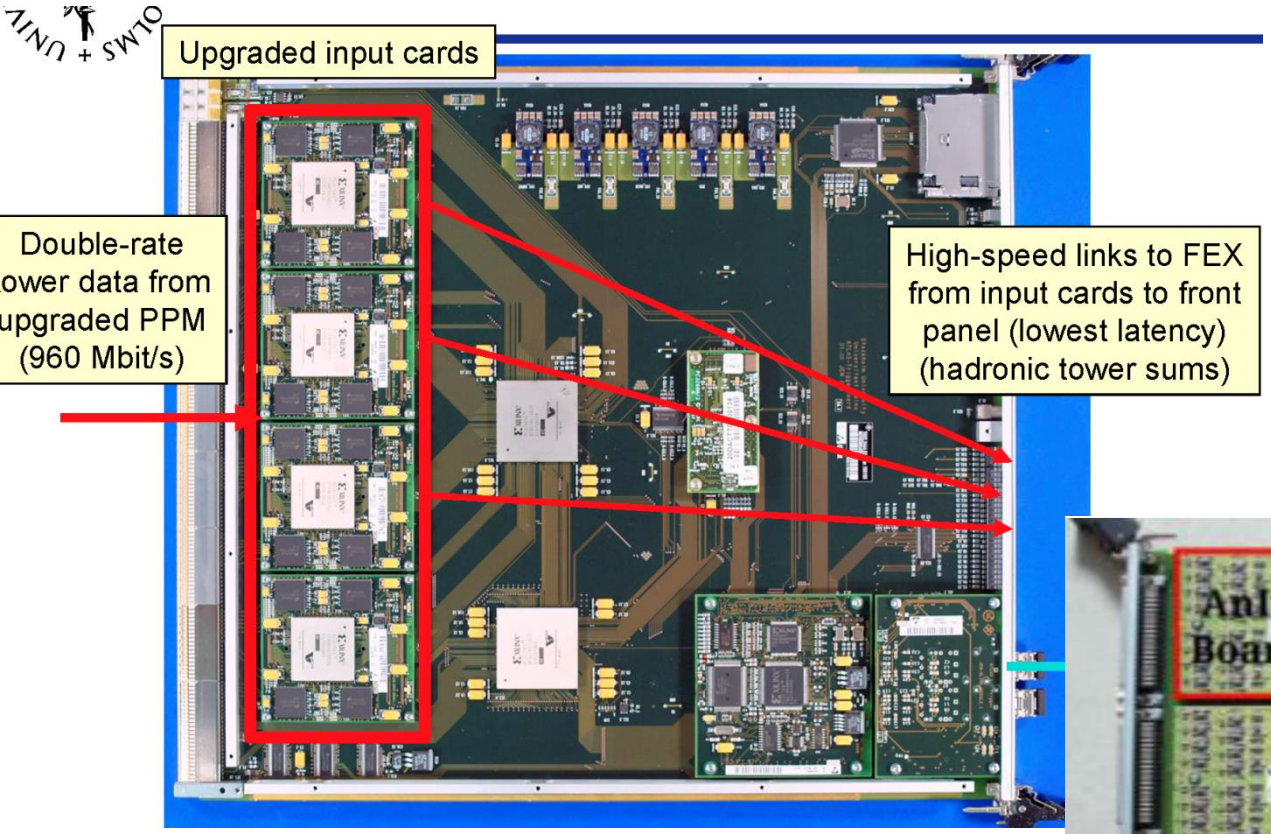
Tilecal o/e converters

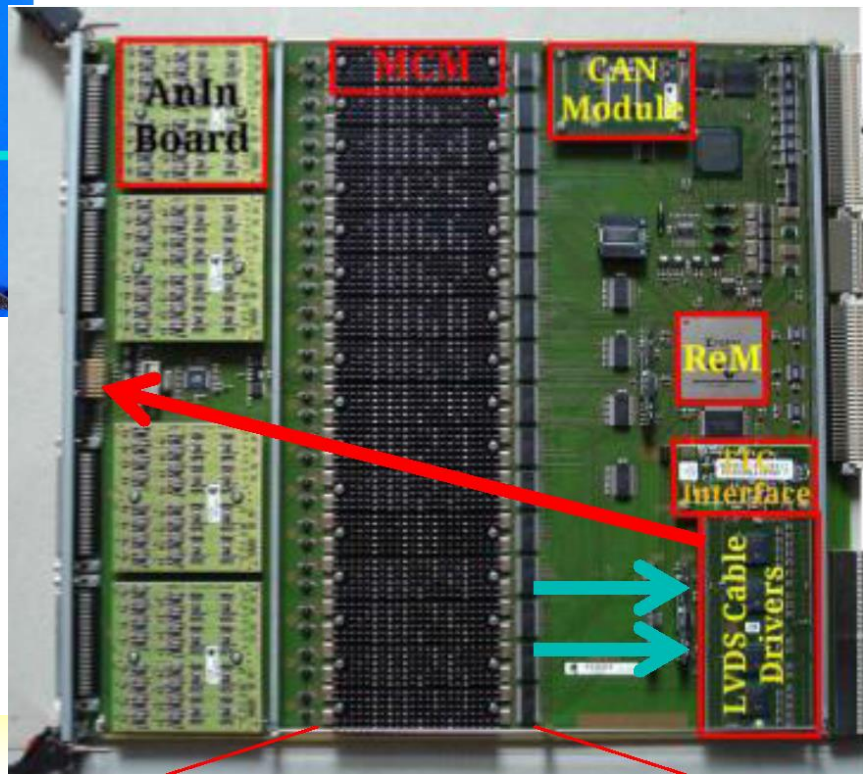
- https://indico.cern.ch/getFile.py/access?contribId=101&sessionId=8&resId=1&materialId=slides&confId=158040

Alternatives



The two L1Calo based options (2, 3)





Option 2: PreProcessor

- Minimal latency:
  - Essentially equal to option 1;
- Can extend dynamic range:
  - nMCM can drive outputs at higher rates, so more bits per tower possible
  - 'Easy' to get 9 bits, 10 bits probably possible
- Relatively low cost
  - nMCM will already exist
  - A few (small) LVDS link boards
  - Possibly need to replace some PreProcessor mother boards (8 layers, low component count)
- Low disruption: Only upgrading existing boards

Option 3: JEM upgrade

- Higher latency:
  - Serial transmission from PPr to JEP adds multiple BCs to latency
- Limited dynamic range:
  - BCMUX protocol consumes some bandwidth
  - 9 bits possible (by removing parity), 10 bits probably not possible
- Similar cost to Option 2
  - PreProcessor nMCM and link cards still get replaced (but not PPr mother boards?)
  - Plans to upgrade JEM daughter boards anyway
- Low disruption: Again, similar to Option 2

Option 2 favored over 3

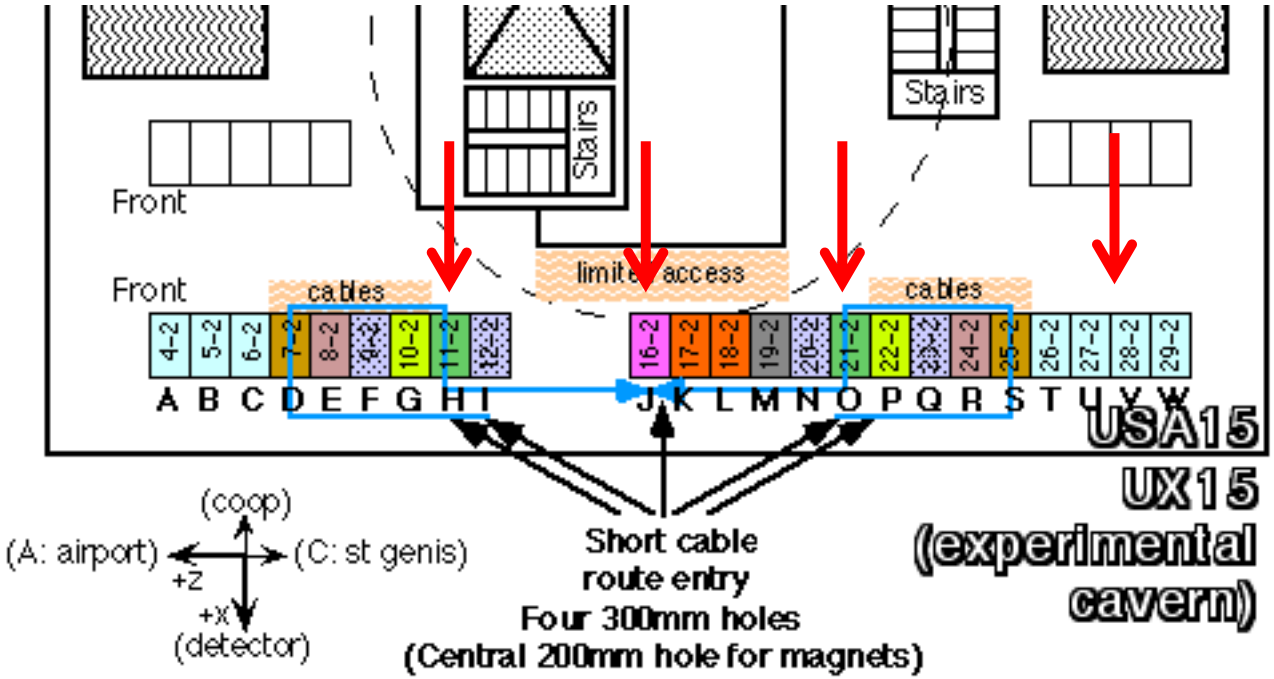
- Lower latency
- Fewer boards in the hardware chain
  - Everything on the PreProcessor
- Easier to expand/change dynamic range
- When would we use option 3?
  - Only if we can't get optical data out of the PreProcessor directly.
  - Options being considered…no show-stoppers seen yet

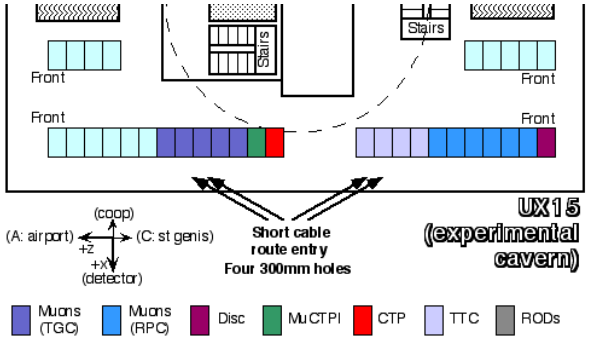
Cable/fibre routing USA15

For phase-1 with FEX:
Route analogue data
via PPr-JEM-FEX
Or rather PPr-FEX ?

Latency ?!?!

Route via JEM needs
to go up and down
twice (rack-false
floor)





Where are the DPS ?

Latencies (from "Report of the ATLAS Calorimeter & Trigger Working Group")

LAr + L1Calo

		BCs	Sub Total	Total
LAR Analog (TTB+Receivers)				
	Time-of-flight to endcap at eta = 2	0.6		
	Cable to pulse preamplifier	1.2		
	Pulse preamplifier and shaper	0.4		
			2.2	2.2
	Pulse peaking time	2		
	Cable to tower-summation board	0.2		
	Analog summation	0.4		
	Cable to USA15 (70 m)	14		
	Receiver station			
	Cable via patch panel and PPM	3.4		
			20	22.2
L1Processors				
In parallel w. jet/Et finding	PPM (preprocessor for e/gamma, tau/hadror	14		
	LVDS Cable to CPM (11m)	2.2		
	CPM (cluster processor module)	13.5		
	CMX (updated CP CMM, excluding serializers	8		
			37.7	
In parallel w. e/g, t/h	PPM (preprocessor for jet, Et)	15.5		
	LVDS Cable to JEMs (11m)	2.2		
	JEM (jet Et processor module)	7.5		
	CMX (updated J/E CMM, excluding serializers	9		
			34.2	59.9
	Cable to CTP (11m) for trigger sums	2.2		
	CMX Output Serializers	2		
	Optical Fibers to L1Topo (11m)	2.2		
			4.2	64.1

LAR System Upgrade Scenario 1 (L1 only)

		BCs	Sub Total	Total
LAR Analog + Digital (LTDB+DPS)				
	Time-of-flight to endcap at eta = 2	0.6		
	Cable to pulse preamplifier	1.2		
	Pulse preamplifier and shaper	0.4		
			2.2	2.2
	Pulse peaking time	0		
	Digitization on LTDB	7		
	Multiplexing on LTDB	1		
	Serializer on LTDB	2		
	Optical cable (70 m) from LTDB to DPS	14		
			24	26.2
	Deserializer on DPS	2		
	Channel demultiplexing on DPS	1		
	Pedestal subtraction	1		
	E, t, Q, N-tap FIR, BCID	5		
	Digital summation	2		
	Multiplexing on DPS	1		
	Serializer on DPS	2		
	Optical cable (15 m) from DPS to FEX	3		
			17	43.2
FEX				
	Deserializer on FEX	2		45.2
	Data duplication between FPGAs	0.5		45.7
	Channel demultiplexing/synchronization	1		46.7
	Primitive processing (e/gamma, tau/hadron, jet, E	5		51.7
	Multiplexing	1		52.7
	Serializer	2		54.7
	Optical cable (10m) to L1Topo	2		56.7
			13.5	56.7

		BCs	Sub Total	Total
L1Topo				
	L1Topo Input Deserializers	2		
	Synchronize to local clock	0.5		
	Algorithmic Processing	1		
			3.5	
	Electrical Output to CTP	0.5		
	Eectrical Cable to CTP (2m)	0.4		
			0.9	
	Output Serializers for optics (if used)	2		
	Fibrest to CTP (if used) (2m)	0.4		
			2.4	
			5.9	70
CTP				
	CTP Input Delay		**2.6**	**72.6**
	Last Electrical Signal arrival			
	CTP_In processing + PITbus	3		
	Last Input Data available for processing			
	New CTP_CORE: processing and outpu	2		
	CTP Out	2.5		
	Cable to LTPi (10m)	2		
	LTPi+LTP+TTCvi+TTCex	2		
	Variable Delay	2		
			13.5	**86.1**
	Fibers to FE electronics (110m)	22		
	TTC Receiver	4		
			26	112.1
TOTAL				**112.1**

Figure 13.3. Detailed estimates of the L1 latency budget in Phase-I

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What is the latency of the PPr / JEM path wrt the Lar DPS path ?

latencies

LAr + L1Calo

	BCs	Sub Total	Total
LAR Analog (TTB+Receivers)			
Time-of-flight to endcap at eta = 2	0.6		
Cable to pulse preamplifier	1.2		
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???

+3

+3

LAR System Upgrade Scenario 1 (L1 only)

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Time-of-flight to endcap at eta = 2	0.6		
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Pulse preamplifier and shaper	0.4		
		2.2	2.2
Pulse peaking time	0		
Digitization on LTDB	7		
Multiplexing on LTDB	1		
Serializer on LTDB	2		
Optical cable (70 m) from LTDB to DPS	14		
		24	26.2
Deserializer on DPS	2		
Channel demultiplexing on DPS	1		
Pedestal subtraction	1		
E, t, Q, N-tap FIR, BCID	5		
Digitial summation	2		
Multiplexing on DPS	1		
Serializer on DPS	2		
Optical cable (15 m) from DPS to FEX	3		
		17	43.2

41.4 + opt cable

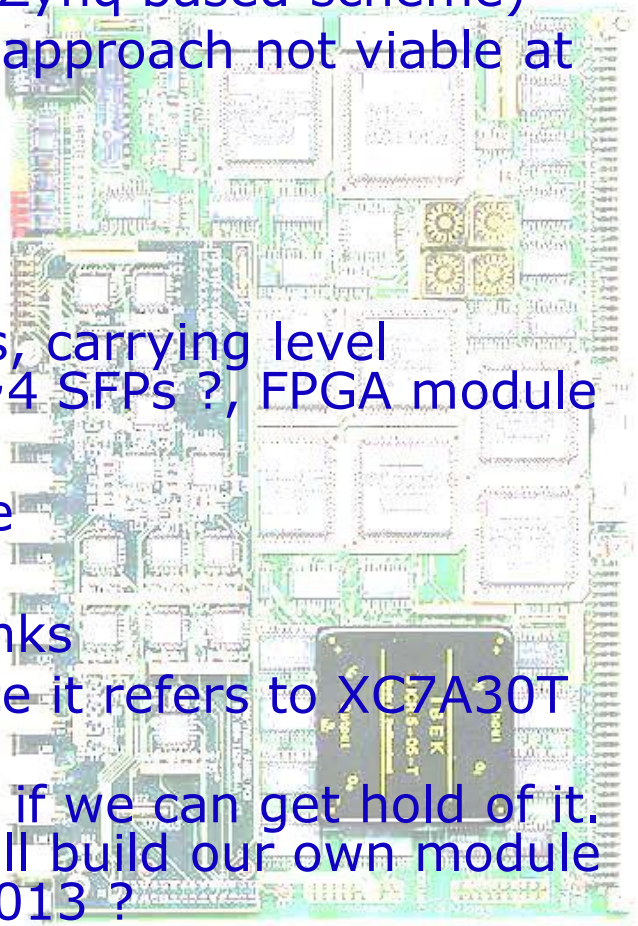
FEX		
Deserializer on FEX	2	45.2
Data duplication between FPGAs	0.5	45.7
Channel demultiplexing/synchronization	1	46.7
Primitive processing (e/gamma, tau/hadron, jet, E	5	51.7
Multiplexing	1	52.7
Serializer	2	54.7
Optical cable (10m) to L1Topo	2	56.7
	13.5	56.7

Latency

- 3 ticks have been assumed for the e/o conversion including serialisation
- Depends on exact data format on incoming electrical stream.
- Larger, if de-serialisation to 40 Mb/s required
- Slightly smaller if data can be packed into 320Mb/s words on-the-fly
- Possibly even smaller if going to more than the baseline rate of 6.4Gb/s
- Optical cable length probably 3 ticks.
- PPM nMCM specs talking about 16 ticks for MCM and nMCM ! (previous slide: 14 / 15.5)
- Where are the DPS ? Is their 15m fibre length realistic ?
- F. Lanni: assumes that DPS path has higher latency than PPr path

VME extender/serialiser

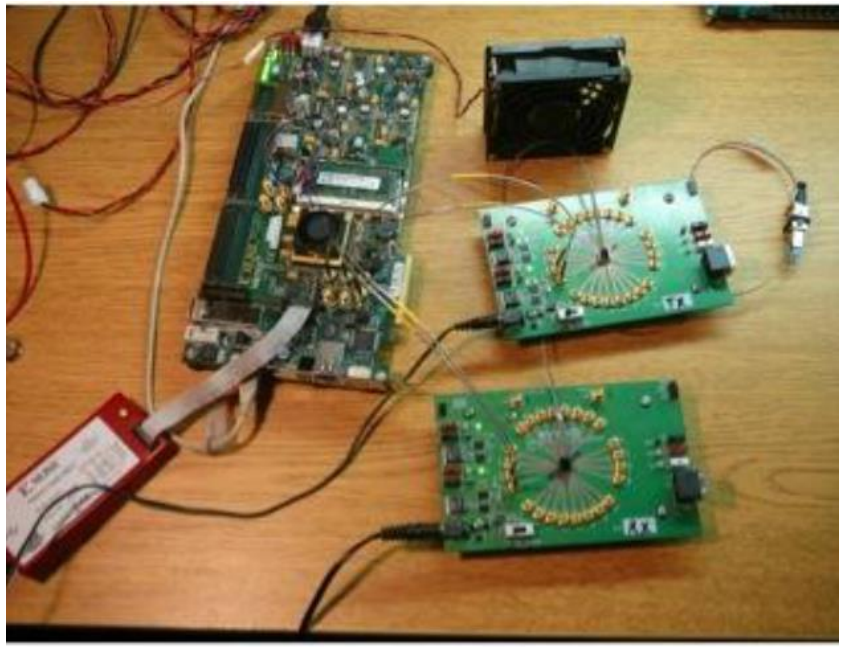
- GOLD (and early L1Topo) module control via a chain 9U-crate CPU → BLT → GOLD (fibre, 1-2Gb/s) (Andreas)
- Long term replacement by Ethernet control (2014 ?) → IPBus workshop next week (Bristol) (or Zynq based scheme)
- Need medium term solution, since 9U/BLT approach not viable at CERN (early system tests)
- Build 6U VME extender
  - 6U VME module
  - Daughter module concept ?
  - Almost passive 6U mainboard ~4 layers, carrying level translators, possibly a CPLD (XC95?), ~4 SFPs ?, FPGA module
  - Enclustra Mars AX3 ?
    - SO-DIMM form factor seems suitable
    - VME slot width ~20mm
    - Not sure about availability of MGT links
    - Documentation seems outdated since it refers to XC7A30T which has been withdrawn by Xilinx
  - Let's try and design for the AX3 pinout, if we can get hold of it. If Enclustra aren't able to deliver, we will build our own module (production silicon available from Jan.2013 ?
  - Reinhold (h/w) + NN (A.R. ? h/w, f/w)… → start now !



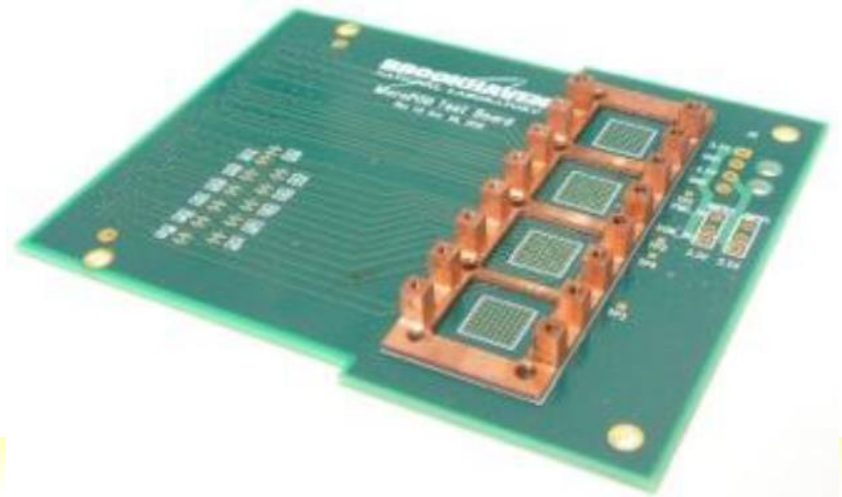
Other…

http://www.mcc-us.com/iportfaq.htm

- IPORT : Tools to control I2C from a PC (for lab / debug purposes)



- Other people are already working on microPOD
- Evaluation board
- Test board BNL



- Uli away (Nov. 27-29) for IPBus workshop !