Level-1 Calorimeter Trigger Phase-I Upgrades

Report of the ATLAS Calorimeter & Trigger Working Group

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the ATLAS Calorimeter & Trigger Working Group

ABSTRACT: The Calorimeter & Trigger (C&T) working group has been mandated by the LAr, Tile and TDAQ Project Leaders in December 2011 to understand the implications of upgrading the calorimeter level-1 system with higher granularity and higher precision information, and with the possibility of deploying more powerful algorithms for the electron selection and the rejection of background jets during the ATLAS operations in Phase-I ($\mathscr{L} \simeq 3 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$) and beyond.
This reports summarizes the conclusions of the C&T working group, laying out the foundation of the future upgrade projects, reviewing the topics agreed by the communities of the three subsystems, and also pointing out where further studies are needed to reach a consensual design.

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Executive Summary

After the planned LHC shutdown LS2 in 2018, the luminosity in ATLAS is expected to exceed the design luminosity by a factor of three. The Level-1 (L1) trigger rate will not be allowed to exceed 100 kHz, since it will require major upgrades of the front-end readout of most subsystems. This imposes a major constraint on the performance of the Level-1 trigger and single lepton thresholds would have to be raised at levels that impact extensively physics acceptance in processes at the electroweak scale.

The usage of higher granularity information at L1 from the calorimeters has been proven by preliminary studies to be an important mitigating factor since it increases the background jet rejection.

There are several possible options to upgrade the L1 calorimeter trigger, and a working group was formed by the Project Leaders of Liquid Argon (LAr), TileCal and TDAQ to analyze them, identify their major issues and risks, and come up with a set of recommendations for the architecture.

This section of the report summarizes the findings and the recommendations of the C&T working group (WG), together with open points of attention, which needs to be addressed and answered before the approval of the upgrade projects of the systems involved.

Findings and recommendations

- **Need of upgrades vs. 'do-nothing' option**

  Refs. [1]- [2] show the predicted rates expeted during operations after LS2. Preliminary shower shape algorithms using increased granularity calorimeter information have demonstrated an effective reduction of the rates from QCD jets, while maintaining fully efficient selectivity of electrons. Risks related to the installation and the commissioning of the proposed system by the end of the LS2 shutdown are moderate (see next bullet). We acknowledge the need for the Phase-I upgrades and we recommend to move forward to the definition and the specification of the system.

- **Digital only vs. Analog and Digital**

  We have evaluated the pros and the cons of implementing the Phase-I upgrade digital only system. The existing Level-1 calorimeter (L1Calo) trigger required an extensive period of time between construction, installation and commissioning. A similar effort for a fully new L1Calo would not be compatible with the duration of the LS2 shutdown and risks would be too high. We fully endorse the decision to develop a solution that allows ATLAS to maintain the existing L1Calo system and to integrate it with the new higher granularity and higher precision digital elements. This strategy allows for better flexibility in the future phases, for possibilities of staging, and for an "adiabatic" integration in ATLAS.

- **Front-End: separation between functionalities**

  Operating side-by-side in the Front-End crates the "legacy" analog trigger builder boards (TBBs) and the "new" LAr Trigger Digitizer Boards (LTDBs) seems feasible. We recommend to use this approach as baseline design for the E.M. calorimeters. In the HEC and FCAL detectors the trigger driver boards (TDB) are relatively sparesely populated and both options (single mixed analog/digital board or two separate boards) are possible. The overall complexity of the front-end system in the two cases will determine what is the optimal solution. Such a decision can in any case be made at a later stage.

- **Granularity of the E.M. calorimeters**

Ref. [3] summarizes the configuration and the granularity of all the LAr calorimeters. The trigger information from the E.M. calorimeters could be based on the so-called "1441" scheme (i.e. the number of Super-Cells element in a trigger tower). Early studies using a shower shape variable showed some sensible but not significant advantage over the "1141" scheme. The 1441 scheme guarantees better flexibility, it allows to implement in future different and better shower shaper algorithms, and it may adapt better to the needs of the calorimeter trigger in Phase-II. For these reasons we recommend it as baseline option.

- **Granularity of the Forward Calorimeters**

  Performance studies should determine how much the forward jet and missing transverse energy trigger will degrade. These studies are not completed at this stage.

  Anticipating the harsh conditions expected for both Phase-I and Phase-II upgrades in the Forward regions, a scheme has been developed to increase the granularity in the FCal1 and FCal2 modules. There are no critical technical challenges, and the impact on the overall costs of the project is very modest. The recommendation of this working group is to include the high granularity FCal scheme in the baseline design. However, we also recommend to prioritize the simulation performance studies for the next steps of the upgrade project approval.

- **Granularity of the Hadronic Calorimeter**

  The hadronic calorimeter granularity in η, ϕ is fixed by the construction both in the TileCal and in the LAr HEC modules. Studies on jet trigger turn-on curves and on the hadronic veto in the electron triggers convincingly indicate that there is no clear benefit in using the hadronic calorimeter longitudinal segmentation rather than the the full hadronic trigger tower. We don't recommend to use layer information from the hadronic calorimeters at L1.

- **TileCal D-layer**

  Dedicated D-layer outputs are available at the trigger patch panel in USA-15. The reason for this was their potential use for supporting muon identification. The value of confining the muon track to a given D-cell or via the time of flight between the D-cell and registration in the muon detector is probably marginal ($\simeq$ 2mm would be needed) but needs to be studied. The advantage of using D-cell data to sharpen trigger turn-on curves has been shown to be negligible (see above). Unless new contradictory results are produced it seems unlikely that the D-cells will be used to enhance the trigger.

- **Latency budget**

  The routing of the new digital signals introduce extra–latency. Preliminary estimates are consistent with the ATLAS overall latency budget: dedicated high rate tests with the existing ATLAS detectors have shown the feasibility of operating the ATLAS detector with an increased L1A latency of 18-20 ticks. The new calorimeter trigger system fits into the budget. However, it is not yet well understood what are the safety margins, in particular because of the constraints on the L1A by the SCT detector. It is therefore very important to further develop the analysis of the overall system, possibly to confirm some of the assumptions made so far with measurements, as soon as the first hardware prototype modules become available. A full analysis of the latency budget should be among the top priorities of the systems in preparation of their TDRs.

- **Compatibility with Phase-II upgrades**

The architecture proposed seems consistent with the current plans for the upgrade of the trigger system in Phase-II. In case of a dual hardware-based first level trigger (L0/L1) the system under consideration would naturally mature in the future Level-0 calorimeter trigger. In case ATLAS will decide for a single Level-1 trigger with extended latency and rates, the system installed in Phase-I could form the core of the trigger input stage for clustering and for the e/γ and jet/E processors. The usage of full granularity information from the calorimeter RODs will build on it, but its performance benefits have to be fully investigated.

Open questions and points of attention

- **ADC resolution and dynamic range**

  Using 12-bit ADC resolution seems a feasible option and should be adopted as baseline design. Truncation to 10-bits may be implemented in the Digital Processing System (DPS) in case it is needed to guarantee the total data throughput.

  Definition of the least significant bit (LSB), or equivalently of the MSB should be derived by physics and performance studies. For algorithms to be implemented in the eFEX there is a consistent advantage of having 64 MeV (or 256 MeV as second choice) precision data. For jet and MET trigger studies, it seems that it 256 MeV (or 512 MeV) would be acceptable. Further investigation is required. While the decision is not a show-stopper, it may impact the design of the TileCal-Feature Extractor (FEX) data interface (see below).

- **Organization of the fibers between the DPS and the FEX systems**

  To provide sufficient 'environment' for sliding window algorithms, each FEX system will typically require two copies of each link from the DPS's FPGAs. The preferred solution is to have four parallel sets of optical transmitters for each output, two for each FEX. For technical reasons, the eFEX partitioning may require an additional two-fold duplication of some digital input links. It is not yet decided how this additional duplication should be implemented.

  Considering the early stage of development, no recommendation is given by this working group at this moment, on how this information duplication should be implemented technically. Specification of the interfaces, organization of the fibers, data bandwidth and transmission protocols (see also next item) are being evaluated.

- **Data protocols: BCMuX and alternatives**

  A time multiplexing protocol (BCMuX) is used in the existing L1 data-path between the Pre-Processor and the Cluster Processor modules that allows two channels to be read out on the same link in two consecutive bunch crossings, essentially halving the number of links necessary.

  The currently planned eFEX architecture relies on such a reduced link count between the DPS and eFEX, and the L1Calo group strongly favor the implementation of a similar BC-Mux scheme for this purpose. Motivations for this include the fact that BCMuX is simple to implement, has a small protocol overhead, and has a fixed, low latency of a single bunch crossing.

  The BCMuX protocol assumes the use of a BC identification (BCID) algorithm based on a digital filter applied to the raw ADC data over several BCs, followed by a peak finder that identifies BCs where the filter output is a maximum. By using a peak-finder based BCID algorithm, no two consecutive bunch crossings can be non-zero for any channel. Therefore, two neighbouring Super Cells will at most report two non-zero values over two consecutive bunch crossings.

On the other hand, calorimeter groups are investigating different online reconstruction algorithms based on source recovering by the deconvolution of the digitized signals. The algorithms yield energies in the calorimeter Super-Cells at each BC. In this context alternative protocols need to be investigated that also allow for a reduction of link bandwidth without loss in signal sensitivity and background rejection and within the same latency budget.

Montecarlo studies will be performed at the highest expected pile-up rates (HL-LHC conditions), in order to verify the effectiveness of both strategies applied to the smaller geometry of the Super Cells, specifically with respect to the improved object identification of the FEX processors.

No specific recommendation is given by the WG at this time: the studies and the investigations should be concluded relatively early, so that a consensus can be achieved by the time of the Initial Design Review or shortly after, well in advance of the release of a TDR given the significant implications of the design on both the DPS and FEX processors.

- **Data routing from the TileCal to the e/j-FEX**

  Two options are being explored:

  1. L1Calo plans to upgrade daughter boards in the current PreProcessor and Jet/Energy-sum modules to extract the TileCal hadronic tower sums from the real-time data path, and transmit them optically to the two FEX systems.
  2. An alternative recent proposal has been made where the TileCal trigger towers analog signals are fanned out at the level of the patch-panels, digitized and sent to processing boards, mirroring the scheme used for the data routing of the LAr HEC calorimeters digitized signals.

  Both options have advantages and disadvantages, from a technical point of view, and in terms of resources and costs. Further investigation is required to arrive to an agreeable conclusion.

1. Introduction and mandate of the working group

After the planned LHC shutdown LS2 in 2018, the luminosity in ATLAS is expected to exceed the design luminosity by at least a factor of three. However, it is very unlikely that there will be any freedom to increase the Level-1 Accept rate beyond 100 kHz, as doing so requires a major upgrade to all front-end detector components, which is not feasible on this time-scale. This imposes a major constraint on the performance of the Level-1 trigger. If no improvement were possible, it would necessarily imply raising thresholds to the point where they could have a major impact of the physics program. In particular the single electron trigger threshold may cut into the electroweak energy domain in an unacceptable way.

One possible mitigating factor is the possibility to use higher granularity calorimeter information at Level-1, at least in the LAr calorimeters. Full granularity information could not be available without a major upgrade, but some additional information could be provided with a relatively localized intervention on both the calorimeter and trigger system, along with the production of new hardware to process the signals. This extra granularity (between 5 to 10 times the information content for the Liquid Argon EM layer, depending on design choices) has been shown to improve the electron trigger by providing better background jet rejection. Finer granularity may also help to sharpen jet and missing energy thresholds.

However, there are many possible choices of the final system design, and each has implications for time-scale, feasibility with available technology and invasiveness on the current system. One serious constraint is the need for the calorimeter trigger system to be available and reliable as soon as LHC goes back into operations after LS2. A group was set up to study the options, examine the major design issues and come up with a set of recommendations for the architecture. The primary objective is to improve the physics performance within the context of the current system, including latency, engineering possibilities and time-scales. Given the importance of a reliable trigger to the success of ATLAS, the risks and fallback solutions need to be understood. Finally another consideration is the compatibility of this upgrade with the longer term Phase-II upgrade architecture.

2. Architecture options

The three main scenarios a priori were:

1. Do nothing at LS2 and raise trigger thresholds
2. Add an additional digital trigger path with higher granularity information, while maintaining the old signals and trigger system
3. Completely replace the current trigger path with new front-end (digital) signals and build an entirely new trigger system

The impact of raising single lepton thresholds at $\mathscr{L} \simeq 3 \times 10^{34} \mathrm{cm}^{-2} \mathrm{s}^{-1}$ on physics involving W bosons in final states and for a couple of benchmark decay channels for a low mass H boson have been documented in the Phase-I ATLAS Letter of Intent [1].

The solutions for the two calorimeters, LArg and Tile, would not necessarily be the same, as the two projects have quite different architectures and upgrade paths. The need for higher granularity was also not so obvious in the Hadronic layer, though this was also to be studied. Equally other signals not contributing to the electron trigger (e.g. FCAL) needed study to determine if higher granularity was necessary.

For the calorimeters, the design decisions hinge on how and where to produce new trigger signals, and what level of granularity is required. For Liquid Argon, assuming work only at the front-end crate level, the maximum granularity is already defined. However, the best choice of granularity within these options needed to be determined, along with a design that fits the new modules into the current crates. For TileCal, the options were more limited at this stage, essentially comprising the possibility to use the already provided D-layer signals.

Assuming the new trigger system was built, the design concept of the trigger processor would be similar to the current system The need for a better electron trigger means that the most vital part of the new trigger processor would be an electron feature extractor (eFEX) which could perform the new algorithms on a denser set of signals. Between this and the new digital signals coming into USA15 there is a requirement for a system which identifies and calibrates the incoming signals (the DPS). The design is mostly independent of whether the digital signal are sent in parallel with the old analogue signals, or as a replacement. The main difference in the design in this case is the lack of a fallback solution if the analogue signals are removed. Other elements of the trigger processor are the possibility of a jet processor (necessary if no analogue signals, optional otherwise, but may produced an improvement in the trigger turn-ons), and the need to interface with the old analogue system for signals where no digital equivalent exists.

Along with the large scale architecture choices, there are more detailed decisions to make. These include exact definition of the higher granularity trigger 'super-cells', the dynamic range of signals at many points in the system and finally the complete specification of the connectivity. Not all of these details are required on the time-scale of the major architecture decisions, but should be studied for full design specification.

3. Granularity of the EM 'Super-cells'

A few configurations were studied to provide the trigger processors with higher precision and higher granularity data from the EM calorimeters. The detector elements grouped to form a single readout channel for the calorimeter Digital Processing System (DPS) and for the trigger Feature Extractor processors (FEX) are conventionally defined in this report and elsewhere [3] as **"Super-Cells"** (SC). While no significant gain in jet rejection would be achieved using fine segmentation in the presampler and in the 3rd layer of the calorimeter, the granularity of the first and second layer of the E.M. calorimeters has been considered. Two schemes were proposed here identified by the number of Super-Cells for each layer of the calorimeters in each trigger tower (TT).

- **1-1-4-1**: $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ for the presampler, the first and the third layers, $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$ in the second one.
- **1-4-4-1**: $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$ for both the first and second layers.

A slight improvement in electron fake rejection was proven by preliminary studies [**?**] and the fact that a larger flexibility could be achieved in particular if projected to Phase-II pileup conditions ($\mathscr{L} \simeq 5 - 7 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$, i.e. an average min bias interactions per bunch crossing $\mu \simeq 135 - 190$), convinced us to adopt the 1-4-4-1 configuration as baseline. The following two sections will summarize the specific configuration of the barrel and end-cap E.M. calorimeters. More details can be found in an ATLAS INT note [3] under preparation.

3.1 "Super-Cell" configuration in the barrel E.M. calorimeter

Figs. 3.1- 3.3 show the correspondance between the existing TT and SC in the barrel E.M. calorimeter. Each TT is formed by summing the pre-sampler (PS) and the three sampling layers (Front, Middle, Back) of the E.M. calorimeter's layer sums (with $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ area). In

the proposed upgrade configuration the "Super-Cells" are defined as groups of n$\times$m cell in η-ϕ respectively with (n,m)=(4,1), (8,1), (1,4), (2,4) in the PS, Front,Middle, Back respectively.

Above $\eta \geq 1.4$ the E.M. barrel geometry changes. Only two sampling layers are defined with different granularities in η. To handle the geometry's change two regions are defined with different SC configurations as shown in Fig. 3.3. The concept of "region" is derived from the one adopted in the convention of ATLAS identifiers as outlined in [**?**]. A few changes with respect to the conventions for the LAr readout cells in the aforementioned [**?**]: a geometry changes for a specific layer propagates to all the other layers of the same detector (PS included); the η,ϕ indices are not reset when entering a new region of a specific detector. Notice the PS region 1 ends with a "narrower" cell (η=1.5-1.52). Whether this is summed to SC=14 or kept as separate SC still has to be decided. Currently the cell is not integrated in any TT.

3.2 "Super-Cell" configuration in the end-cap E.M. calorimeter

The end-cap E.M. calorimeters have a more complex intrinsic geometry, in particular with the first sampling changing patterns along η both in the outer and the inner wheels, and the presampler covering only between $1.5 \leq \eta \leq 1.8$. In terms of SCs geometry 7 regions have been identified as shown in Figs. 3.4- 3.6. Again Ref. [3] contains more details on each of the 7 regions.

3.3 "Super-Cell" summary tables for the E.M. calorimeters

Table 3.1 summarizes for each of the E.M. calorimeters the organization of the Super-Cells, their granularity in η/ϕ and the summing multiplicity required from the individual calorimeter cells implemented in the Front-end electronics.

Region	Eta Range	Sampling Layer		Cell	"Super-Cell"				
		Name	Index	Granularity	n$\times$m	$\Delta\eta$	$\Delta\phi$	η-index	ϕ-index
E.M. Barrel (EMB)									
0	0 - 1.4	Presampler	0	0.025$\times$0.1	4$\times$1	0.1	0.1	0-13	0-63
		Front	1	0.003125$\times$0.1	8$\times$1	0.025	0.1	0-55	0-63
		Middle	2	0.025$\times$0.025	1$\times$4	0.025	0.1	0-55	0-63
		Back	3	0.05$\times$0.025	2$\times$4	0.1	0.1	0-13	0-63
1	1.4 - 1.52	Presampler	0	0.025$\times$0.1	5$\times$1	0.12	0.1	14(-15)	0-63
		Front	1	0.025$\times$0.025	8$\times$1	0.025	0.1	56-58	0-63
		Middle	2	$\simeq$0.075$\times$0.025	1$\times$4	$\simeq$0.075	0.1	56	0-63
E.M. End-cap (EMEC)									
0	1.375 - 1.5	Front	1	(1$\otimes$0.05$\oplus$3$\otimes$0.025)$\times$0.1	4$\times$1	0.125	0.1	0	0- 63
		Middle	2	(1$\otimes$0.05$\oplus$3$\otimes$0.025)$\times$0.025	1$\times$4	0. 05, 0.025	0.1	0,1-3	0-63
1	1.5 - 1.8	Presampler	0	0.025$\times$0.1	4$\times$1	0.1	0.1	0-2	0-63
		Front	1	0.003125$\times$0.1	8$\times$1	0.025	0.1	1-12	0-63
		Middle	2	0.025$\times$0.025	1$\times$4	0.025	0.1	4-15	0-63
		Back	3	0.05$\times$0.025	2$\times$4	0.1	0.1	0-2	0-63
2	1.8 - 2.0	Front	1	0.1/24$\times$0.1	8$\times$1	0.0333	0.1	13-18	0-63
		Middle	2	0.025$\times$0.025	1$\times$4	0.025	0.1	16-23	0-63
		Back	3	0.05$\times$0.025	2$\times$4	0.1	0.1	3-4	0-63
3	2.0 - 2.4	Front	1	0.00625$\times$0.1	4$\times$1	0.025	0.1	19-34	0-63
		Middle	2	0.025$\times$0.025	1$\times$4	0.025	0.1	24-39	0-63
		Back	3	0.05$\times$0.025	2$\times$4	0.1	0.1	5-8	0-63
4	2.4 - 2.5	Front	1	0.025$\times$0.1	4$\times$1	0.1	0.1	35	0-63
		Middle	2	0.025$\times$0.025	1$\times$4	0.025	0.1	40-43	0-63
		Back	3	0.05$\times$0.025	2$\times$4	0.1	0.1	9	0-63
5	2.5 - 3.1	Front	1	0.1$\times$0.1	2$\times$2	0.2	0.2	36-38	0-31
		Middle	2	0.1$\times$0.1	2$\times$2	0.2	0.2	: 44-46	0-31
6	3.1 - 3.2	Front	1	0.1$\times$0.1	1$\times$2	0.1	0.2	39	0-31
		Middle	2	0.1$\times$0.1	1$\times$2	0.1	0.2	47	0-31

Table 3.1. "Super-Cell" configuration in the LAr E.M. calorimeters

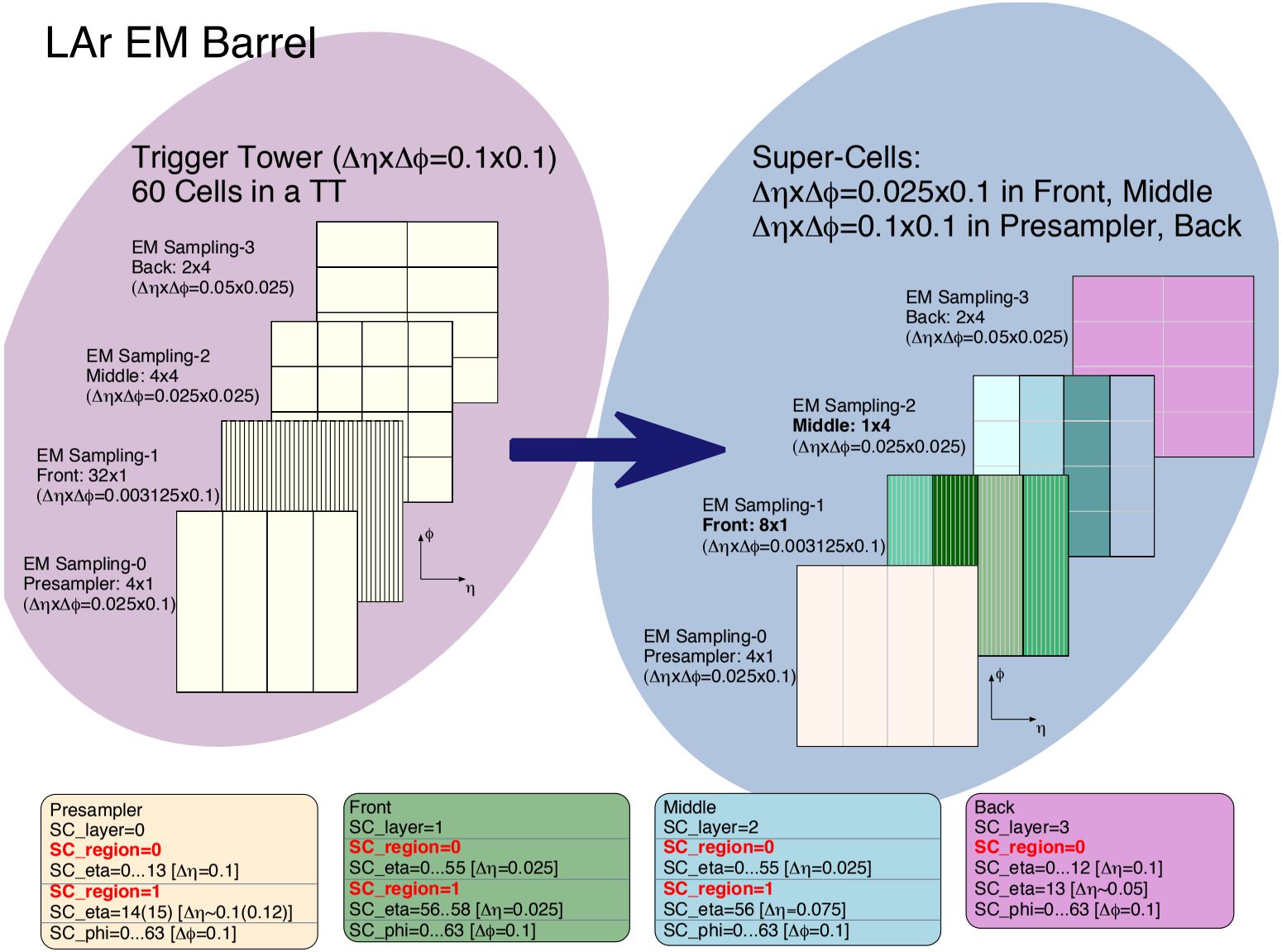

Figure 3.1. “Super-Cell” definition in the LAr E.M. barrel calorimeter

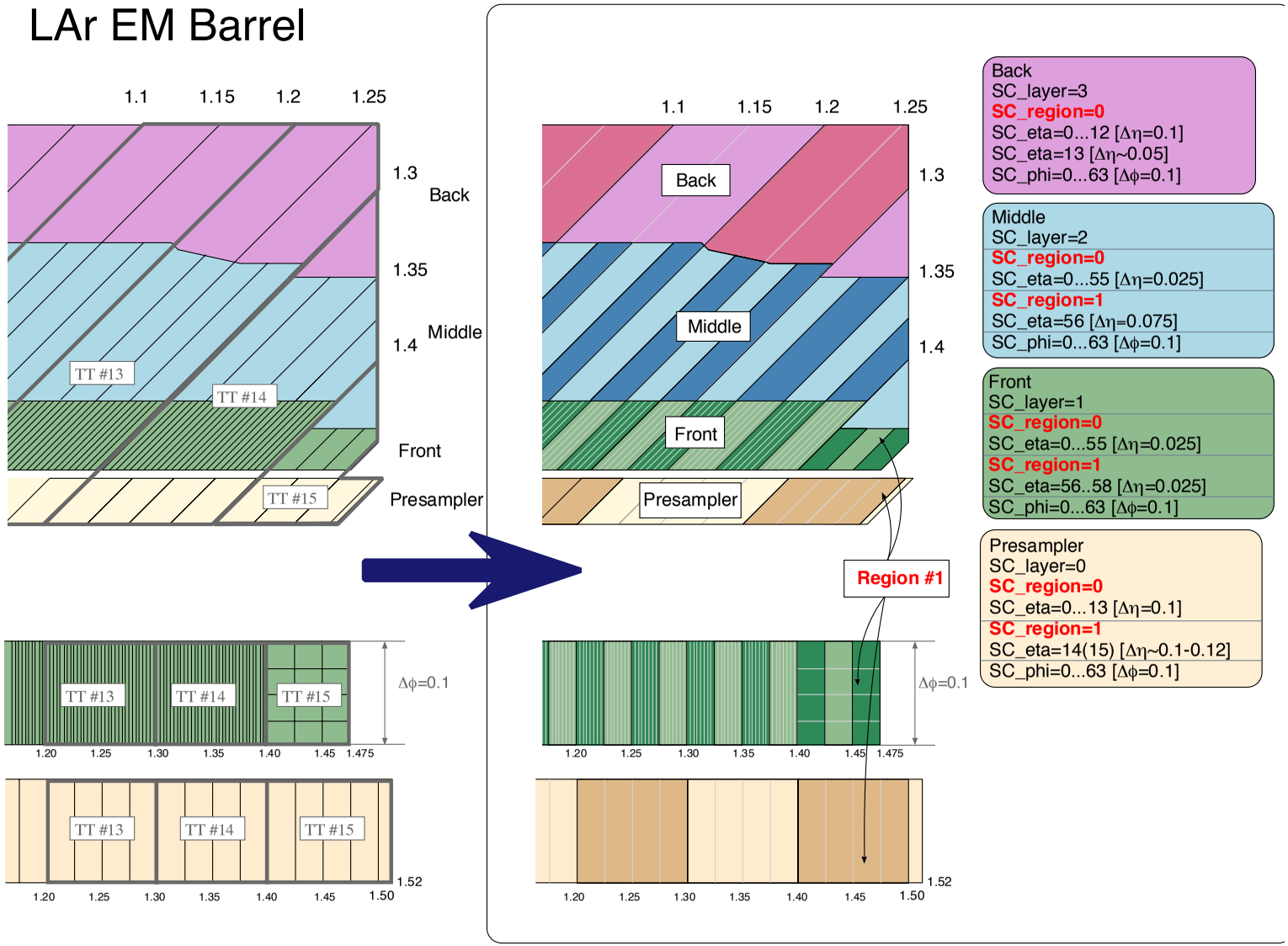

Figure 3.2. Mapping of the “Super-Cells” to the existing Trigger Towers in the E.M. barrel calorimeter

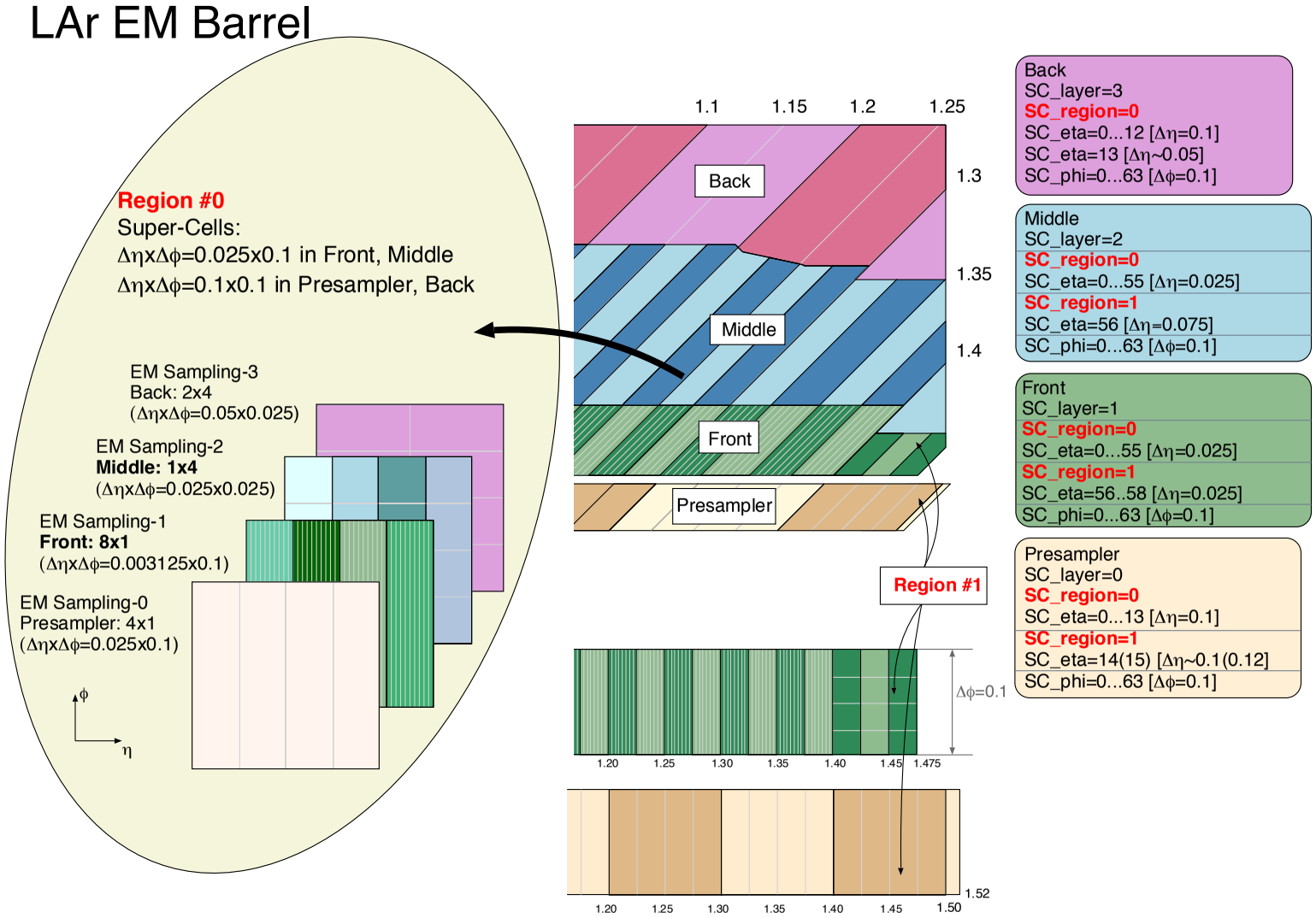

Figure 3.3. Detailed “Super-Cell” definition in the LAr E.M. barrel calorimeter including the barrel end-part

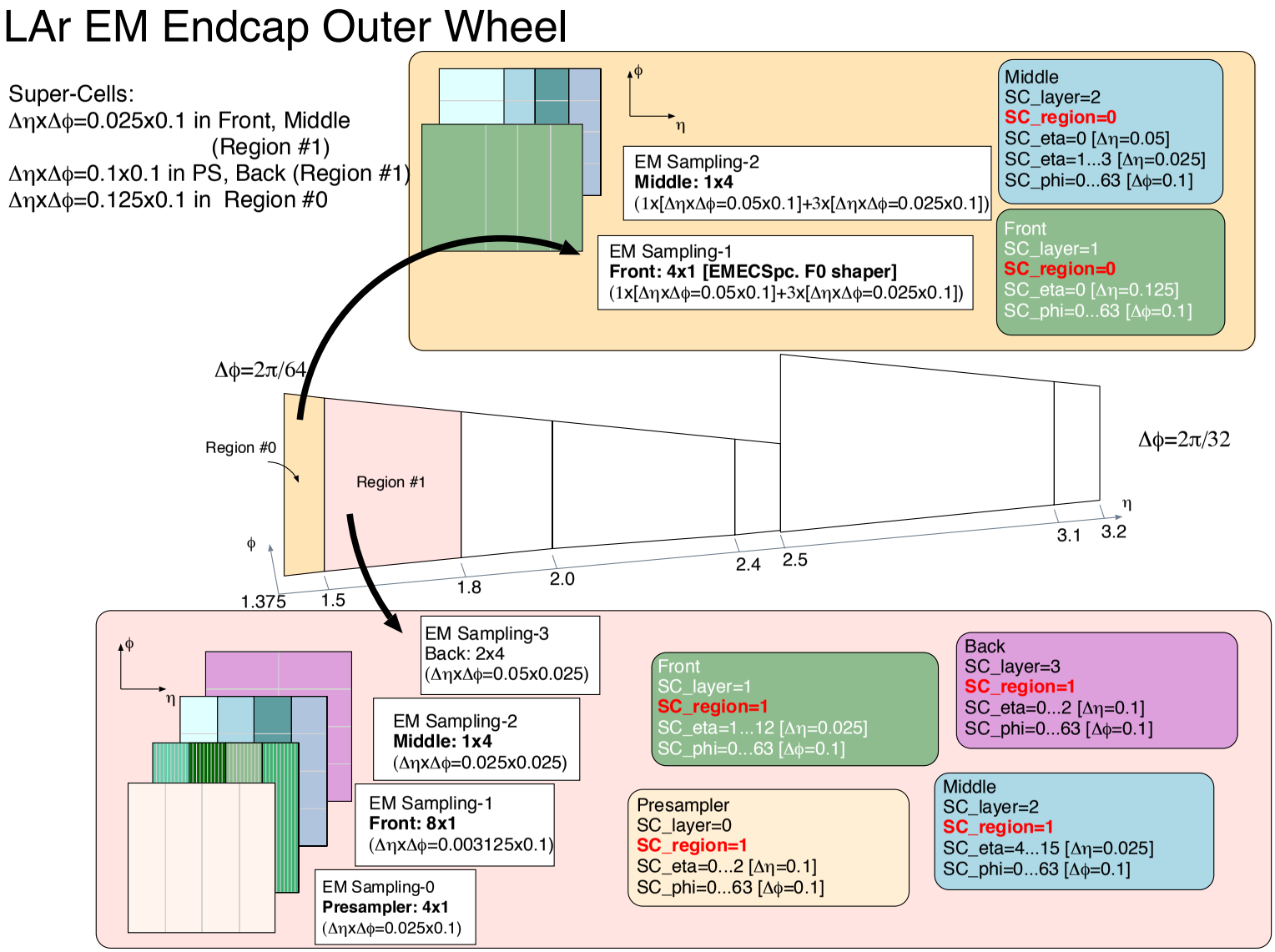

Figure 3.4. "Super-Cell" definition in the LAr E.M. end-cap calorimeter

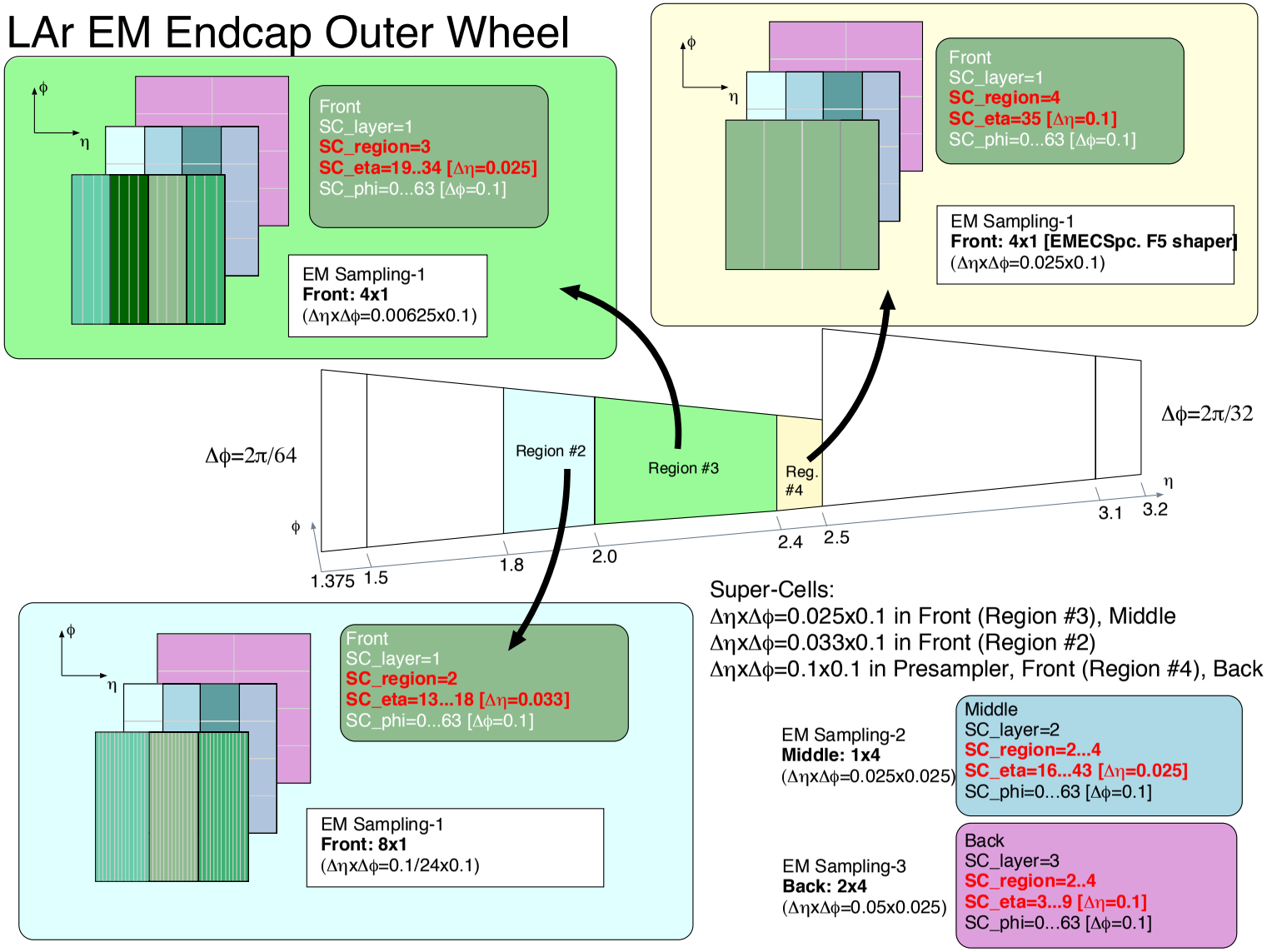

Figure 3.5. Mapping of the "Super-Cells" to the existing Trigger Towers in the E.M. end-cap calorimeter

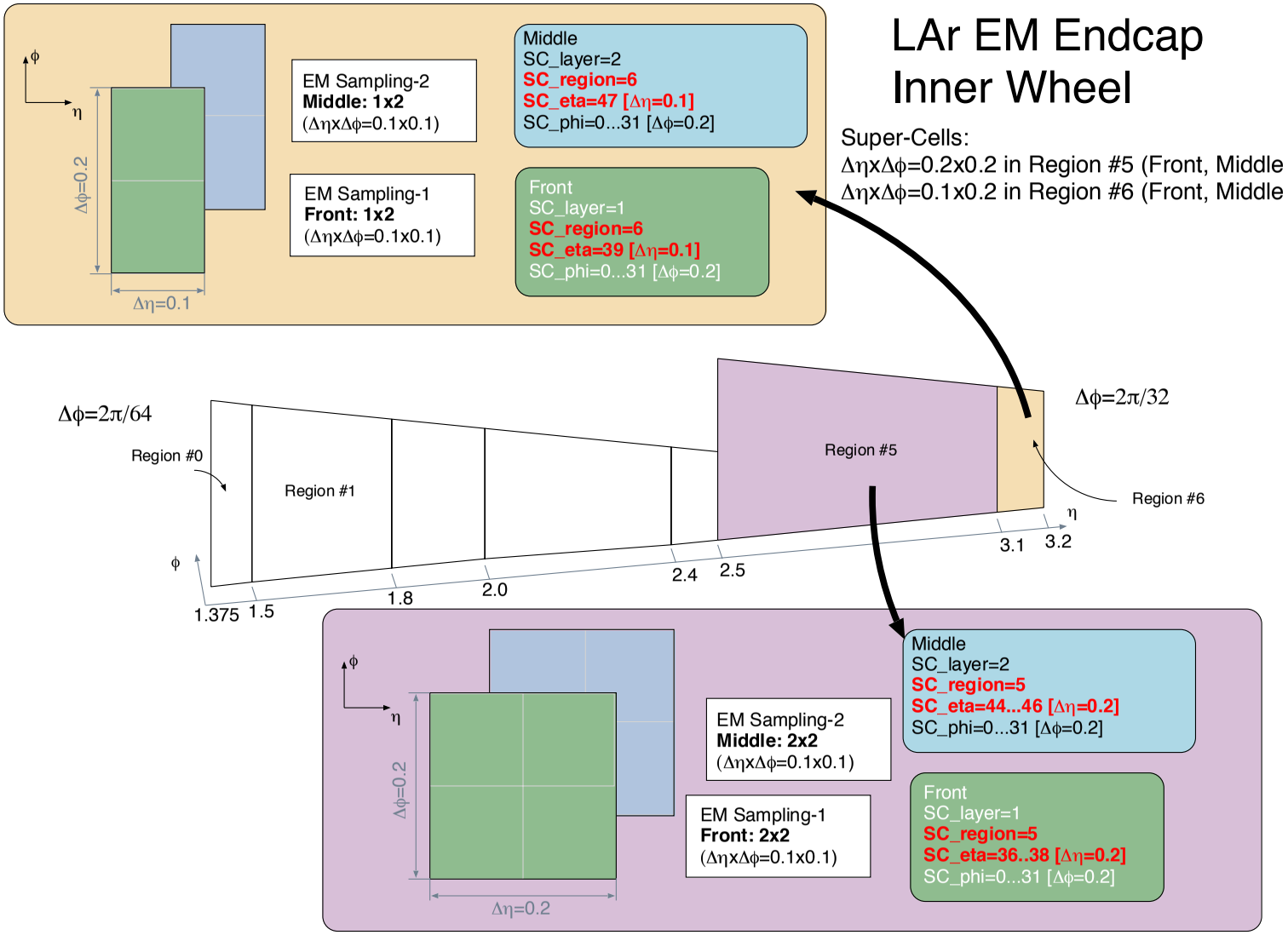

Figure 3.6. Detailed "Super-Cell" definition in the LAr E.M. end-cap calorimeter including the end-cap end-part

4. Granularity in the Hadronic Calorimeter

Information from the hadronic calorimeters are used in both the e-FEX and the j-FEX processors. Studies on jet rejections in electron trigger and jet trigger resolution/turn-ons convincingly indicate that longitudinal segmentation is not improving in a significant way the performance of both the electron and jet triggers at level-1. Furthermore, the transverse segmentation is fixed by construction in the detectors. Therefore we are recommeding as baseline to stay with the tower-size information from the hadronic calorimeters. The question related to the precision of the digital information sent to the e/j-FEX is addressed in Sec. **??**. As for the D-layer see Sec. 6.

4.1 Hadronic veto studies for the Level-1 electron triggers

As discussed in Ref. [2], the inclusion of a hadronic veto to reduce jets faking electromagnetic objects has a significant impact on the trigger rates. This is particularly more relevant if no hadronic isolation is applied in the selections performed presently at the L1. Furthermore, as also indicated in different studies related to the upgrade L1 jet reconstruction (see ahead), it seems reasonable to increase the hadronic tower energy resolution, reducing the present 1 GeV steps to 250 MeV. Table 4.1 presents the results obtained so far to this analysis.

selection criterium	Percentage of (1)	Percentage of (2)
(1) L1 EM $E_T > 23$GeV	100%	-
(2) L1 EM $E_T > 23$GeV Isolated	35%	100%
(3) L1 EM $E_T > 23$GeV Isolated && R_η	15.0%	42.9%
(4) L1 EM $E_T > 23$GeV Isolated && R_η && hadCore	13.1%	37.3%

Table 4.1. Fraction of remaining jets faking L1 EM triggers using the new variable in the EM section (R_η) including present L1 isolation. The numbers are expressed as fractions of the initial number of triggers (1) after a simple threshold or the initial number of isolated triggers (2). For comparison, 98.37% of the L1 matching offline electrons, passing (2) also pass (4).

These numbers were obtained using a $<\mu>=46$ at 14 TeV. The new hadronic isolation (assuming a 250MeV energy resolution of the trigger towers) gives a 5% effect on top of what can be done with the present L1 isolation. In the case of not using any present L1 isolation as described in Table 4.2, the effect of the new hadronic isolation (again, using 250MeV) becomes much more meaningful (13%).

selection criterium	Percentage of (1)
(1) L1 EM $E_T > 23$GeV	100%
(2) L1 EM $E_T > 23$GeV && R_η	28.3%
(3) L1 EM $E_T > 23$GeV && R_η && hadCore	15.3%

Table 4.2. Fraction of remaining jets faking L1 EM triggers using the new variable in the EM section (R_η) not including present L1 isolation.

It is interesting to note that the final numbers with the new hadronic veto are quite similar independent of whether there was or not the present L1 isolation (13.1% or 15.3%). The conclusion that can be taken from here is that the presence of the present L1 isolation becomes irrelevant if the proposed increase of hadronic tower energy resolution can be implemented.

Parallel studies also showed no improvement of the vetoing performance dependending on whether one, two or three hadronic layers were added together. The best case scenario (using only the first hadronic layer) is less than 2% better than the worst case scenario (using the full hadronic tower).

4.2 Inclusive jet and multijet trigger studies

Jet trigger performance in presence of high pileup has been evaluated using the full granularity of the hadronic calorimeters (both TileCal and HEC) The level one hadronic trigger towers are currently built with a resolution of 0.1×0.1 in $\eta \times \phi$ by summing all calorimeter cells in this region. For both the TileCal and the LAr HEC this is achieved by a summing circuits in the front-end electronics. The study used Monte Carlo simulations from $\frac{t}{t}$ events at 14 TeV with μ=46. Efficiency curve turn-ons based on the following algorithms have been compared and analyzed:

- The level one (L1) calculation with 1 GeV resolution is obtained directly from the MC simulation by the standard level-1 trigger reconstruction software in Athena.
- An estimation of the level one curve (EM+HAD) has been also emulated by summing the energies (with infinite resolution) of all the trigger towers in the RoI.
- An alternative calculation of the jet energy has been made by a linear combination from the three hadronic layers in order to profit from the additional hadronic calorimeter depth segmentation. In such way, the energy estimation from jets is performed using Eq. 4.1, where LAr is the energy deposited in the Liquid Argon calorimeter, TileA, TileBC and TileD are the energies deposited in layer A, BC and D from TileCal, respectively, w_1, w_2, w_3, w_4 are the weights and b is the bias. The optimum weights and bias are found using a least square regression and the offline estimated energy as target.

$$E_T^{jet} = w_1 \cdot \sum_{\eta,\phi} E_{LAr} + w_2 \cdot \sum_{\eta,\phi} E_{TileA} + w_3 \cdot \sum_{\eta,\phi} E_{TileBC} + w_4 \cdot \sum_{\eta,\phi} E_{TileD} + b \tag{4.1}$$

- A gaussian filter estimator (EM+HAD-Gaussian) is evaluated by summing LAr and the TileCal trigger towers at the RoI weighted by the Gaussian function with σ=0.4. The gaussian weight is applied in R from the seeding tower in the RoI as shown in Fig. 4.1
- Another estimator is obtained combining the layer weighted sums with the gaussian filter (EM+HAD-Gaussian+LS)

The turn on curves for all methods can be seen in Fig. 4.2 for η covering only the TileCal region. The energy cut was applied at 50 GeV. It can be seen that the L1 (level one with 1 GeV resolution) presents the worse performance, the curve departs from 50 GeV and reaches 100% efficiency around 90 GeV (40 GeV spread). The emulated level one with infinity resolution (EM+HAD) shows better performance, the curve departs from 25 GeV and reaches 100% efficiency around 60 GeV (35 GeV spread). The curve using both Gaussian and depth segmentation is slightly better than the emulated level with infinity resolution being symmetric around the energy cut, the curve departs from 35 GeV reaching 100% efficiency around 70 GeV (35 GeV spread). The results are summarized in Table 4.3.

The turn on curves can be aligned around 50% efficiency (calibration) which can be seen in Figs. 4.3- 4.4 for the regions covered by the TileCal and by the LAr HEC respectively. The L1 curves represents the worse performance, while the others show similar behavior but better performance than L1. It can also be seen that the Gaussian weights improve the turn on curve behavior between 25 and 40 GeV, probably due to the reduction of the pile up effect.

Rise Energy ΔE [GeV]		
Method	10-90%	5-99%
EM+HAD	16	30
EM+HAD-Gaussian	17	27
EM+HAD-LS	14	32
EM+HAD-Gaussian+LS	14	30
L1	20	43

Table 4.3. Turn-on curve rise energy for TileCal.

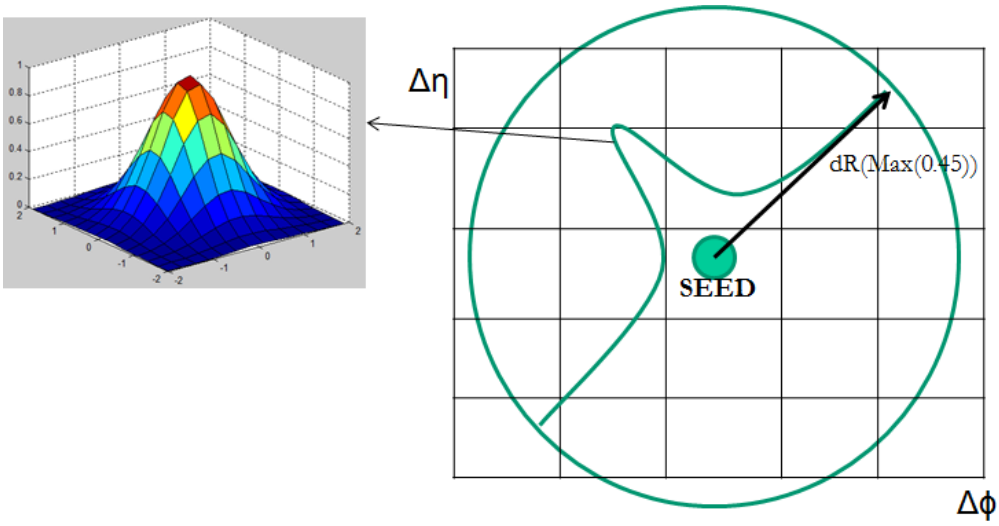

Figure 4.1. Schematic representation of the gaussian weighting filter

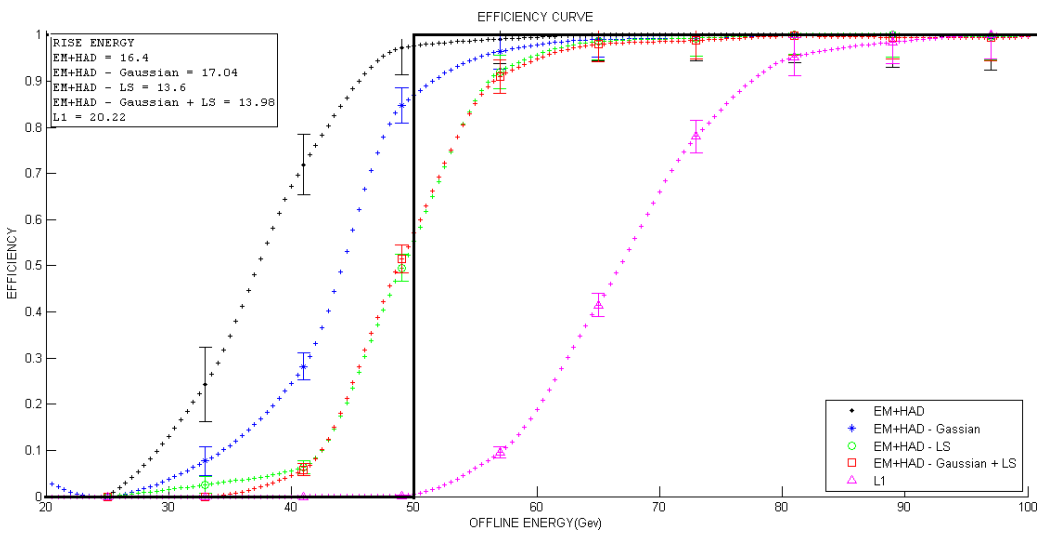

Figure 4.2. Turn on curves for all methods for an energy cut at 50GeV (TileCal region).

The major improvement on the turn on curve for jets is achieved when the energy resolution is increased. However, the use of hadronic depth segmentation based in a linear combination of

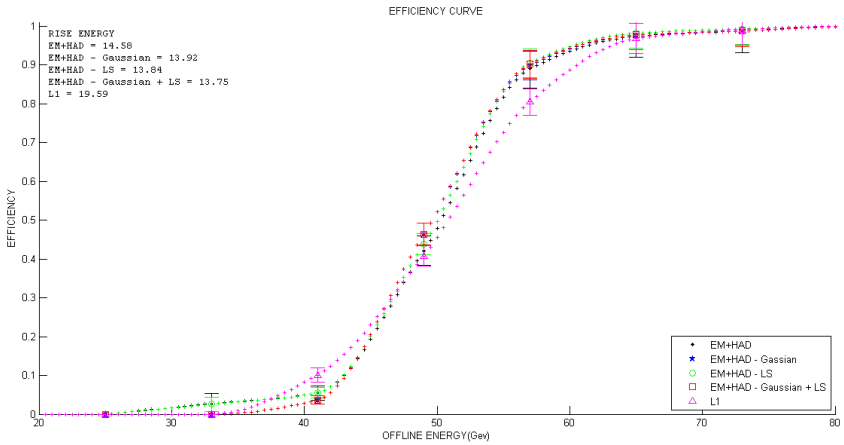

Figure 4.3. Aligned turn on curves for all methods for an energy cut at 50GeV (TileCal region).

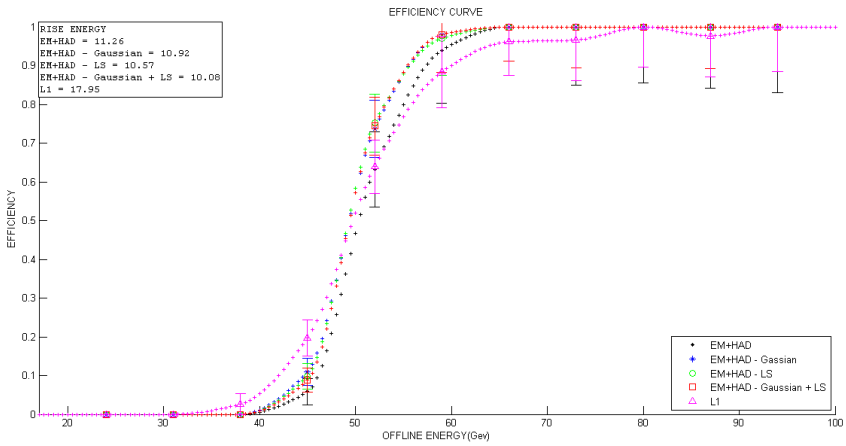

Figure 4.4. Aligned turn on curves for all methods for an energy cut at 50GeV (HEC region).

each calorimeter layer showed negligible effect on the turn on curve for jets. The Gaussian weights improve the behavior of the turn on curve for jets before the energy cut, improving the rejection of unwanted events due to the pile up effect.

From these considerations and from the ones in Sec. 4.1 our conclusion is that there is no need for longitudinal segmentation information at Level-1 from the hadronic calorimeters. What precision (1 GeV or more) of the digitizers is required needs to be studied in detail (see Sec. 7).

4.3 Configuration in the TileCal

TileCal is a cylindrical calorimeter composed of interleaved plastic scintillator and steel tiles. The tiles are organized in 11 concentric layers and divided in 64 azimuthal slices (i.e. along the ϕ-direction), .1 radians each. The calorimeter itself is divided into three parts, the central (long) barrel and two extended barrels. It can also be divided in four partitions, the two extended barrels (EBA and EBC) and two partitions (LBA and LBC) making up the central barrel (see Fig. 4.5). Each scintillator tile is read out via two wavelength shifting fibers, one on each side, $\pm\phi$. The fibers belonging to different cells are grouped together as shown in the figure and each group is read out

by a PMT. Since the two sides are kept apart each cell will be read out by two PMTs creating a twofold redundancy. The cells are in turn organized in three layers A, B (BC) and D. The first two extend 0.1 in pseudorapidity while C takes up 0.2. For the Level-1 trigger the cells are combined in quasi-projective towers where the D-layer signals are split into two. The central barrel will contain trigger towers with $|eta| \leq$1.0 and the extended barrels 0.7$\leq \eta \leq$1.7. Since there is an overlap in the crack region where inner detector and LAr calorimeter services pass through, these will have to be merged outside the detector.

4.4 Configuration in the End-Cap hadronic calorimeter

The HEC towers are formed in the front-end crates shaper ASICs. The pads of the 4 sampling layers are summed in the LM. A "Super-Cell" is equivalent to a trigger tower. As shown in Fig. **??** two regions cover $1.5 \leq \eta \leq 2.5$ and $2.5 \leq \eta \leq 3.3$. The SC sizes in the two regions are $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ and 0.2×0.2 respectively.

Region	Eta Range	Sampling Layer		Cell Granularity	"Super-Cell"				
		Name	Index		n×m	$\Delta\eta$	$\Delta\phi$	η-index	ϕ-index
Hadronic End-cap (HEC)									
0	1.5-2.5	-	0-3	0.1×0.1	4×1	0.1	0.1	0-9	0-31
1	2.5-3.3	-	0-3	0.1×0.1	4×1	0.2	0.2	10-13	0-15

Table 4.4. "Super-Cell" definition in the LAr HEC calorimeters

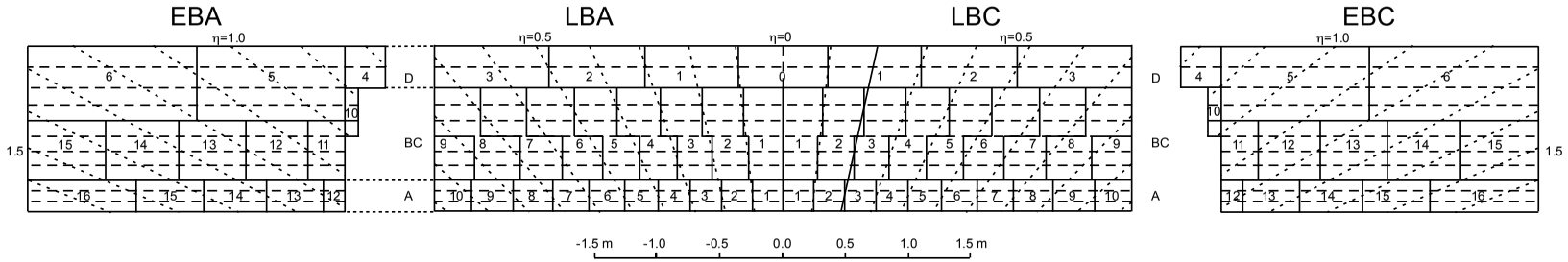

Figure 4.5. Geometry of the Tile calorimeter's trigger towers and layers

LAr Hadronic Endcap (HEC)

Super-Cells (=Trigger Towers)
$\Delta\eta x \Delta\phi$=0.1x0.1 in Region #0
$\Delta\eta x \Delta\phi$=0.2x0.2 in Region #1

Region=0
Pads: P1a,P1b...P19
SC_eta=0...9
[η<2.5, $\Delta\eta$=0.1]
SC_phi=0...63 [$\Delta\phi$=0.1]

Region=1
Pads=P21...P24
SC_eta=10...13
[η>2.5, $\Delta\eta$=0.2]
SC_phi=0...31 [$\Delta\phi$=0.2]

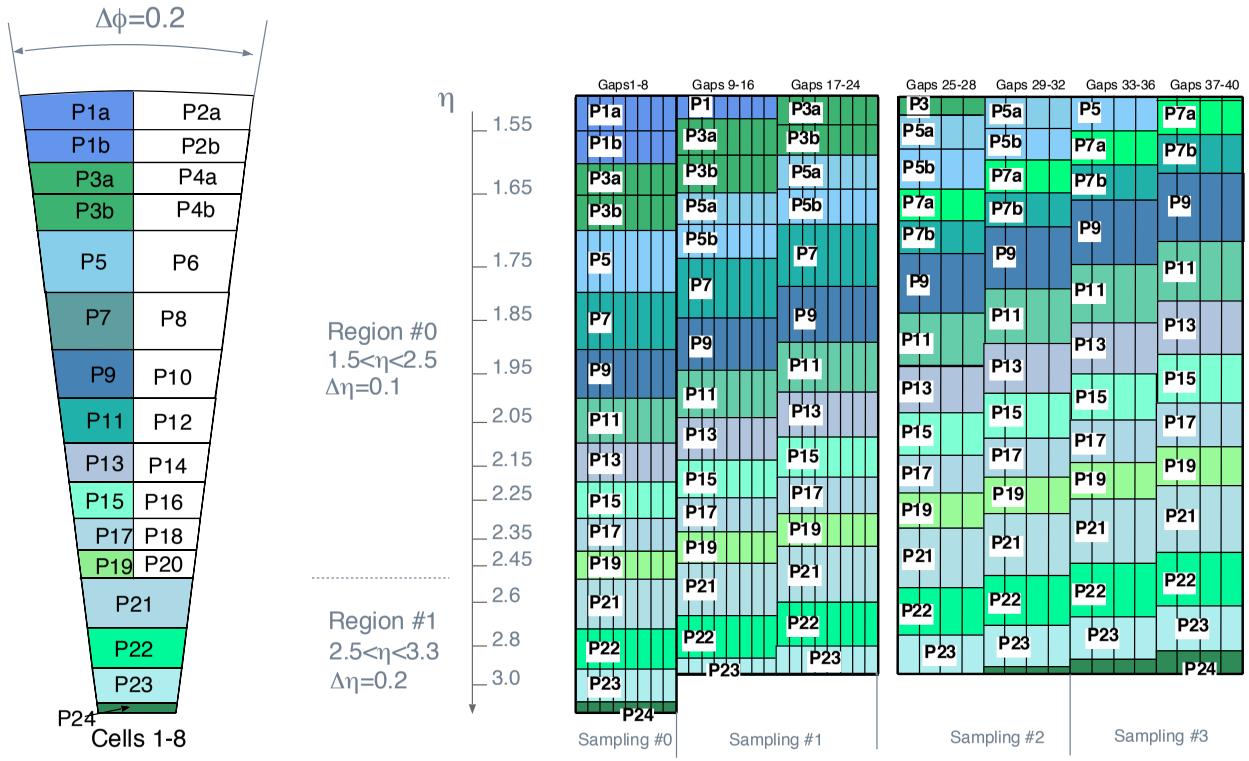

Figure 4.6. “Super-Cell” definition in the LAr hadronic end-cap calorimeter

5. Granularity in the Forward Calorimeter

With the exception of the two outermost η-bins of the FCal-1 module, the SC granularity in the FCal detectors is the maximal achievable by the upgrade of the on-detector LSB in the 14 FEBs in each crate. The FCal modules are built with a non-pointing x-y geometry. Therefore the SC geometry is somewhat irregular in shape and size and only approximate constant $\eta - \phi$ regions can be defined as shown in Figs. 5.1- 5.3 and summarized in Table 5.1.

Region	Eta Range	Sampling Layer		Cell Granularity	"Super-Cell"				
		Name	Index		n×m	$\Delta\eta$	$\Delta\phi$	η-index	ϕ-index
Forward Calorimeter (FCal)									
0	3.1 - 3.2	Fcal-1	0	x,y-various	x,y-various	$\simeq$0.1	0.4	0	0-15
1	3.2 - 3.5			x,y-various	various	$\simeq$0.1	0.4	1-3	0-15
2	4.5 - 4.0			x,y-various	various	$\simeq$0.1-0.15	0.4	4-7	0-15
3	4.0 - 4.9			x,y-various	various	$\simeq$0.15-0.2	0.4	8-11	0-15
0	3.1 - 4.9	FCal-2	1	x,y-various	various	0.1-0.3	0.4	0-7	0-15
		FCal-3	2	x,y-various	various	0.4-0.5	0.4	0-3	0-15

Table 5.1. "Super-Cell" definition in the FCAL LAr calorimeters

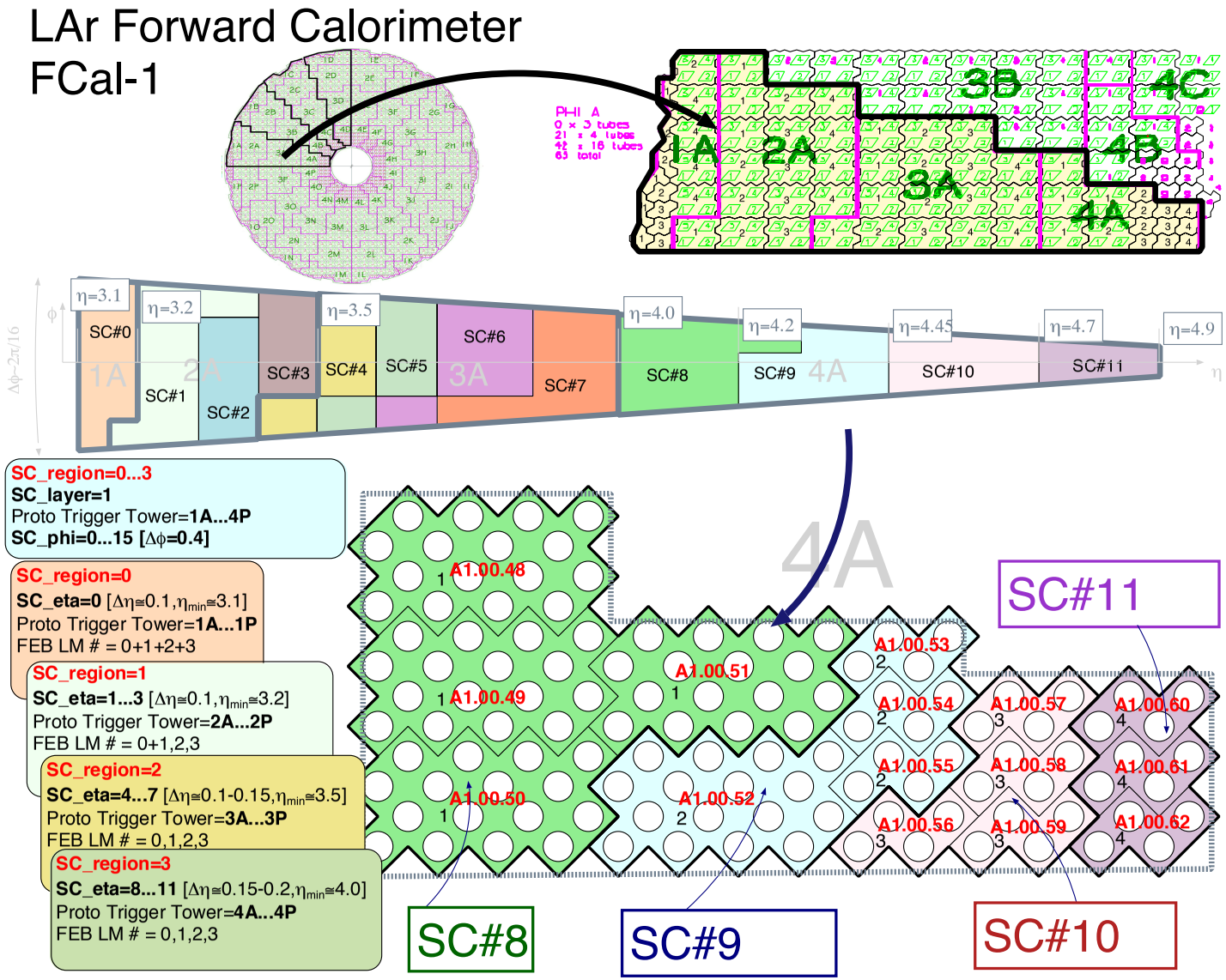

Figure 5.1. "Super-Cell" definition in theLAr forward calorimeter (FCal-1) calorimeter

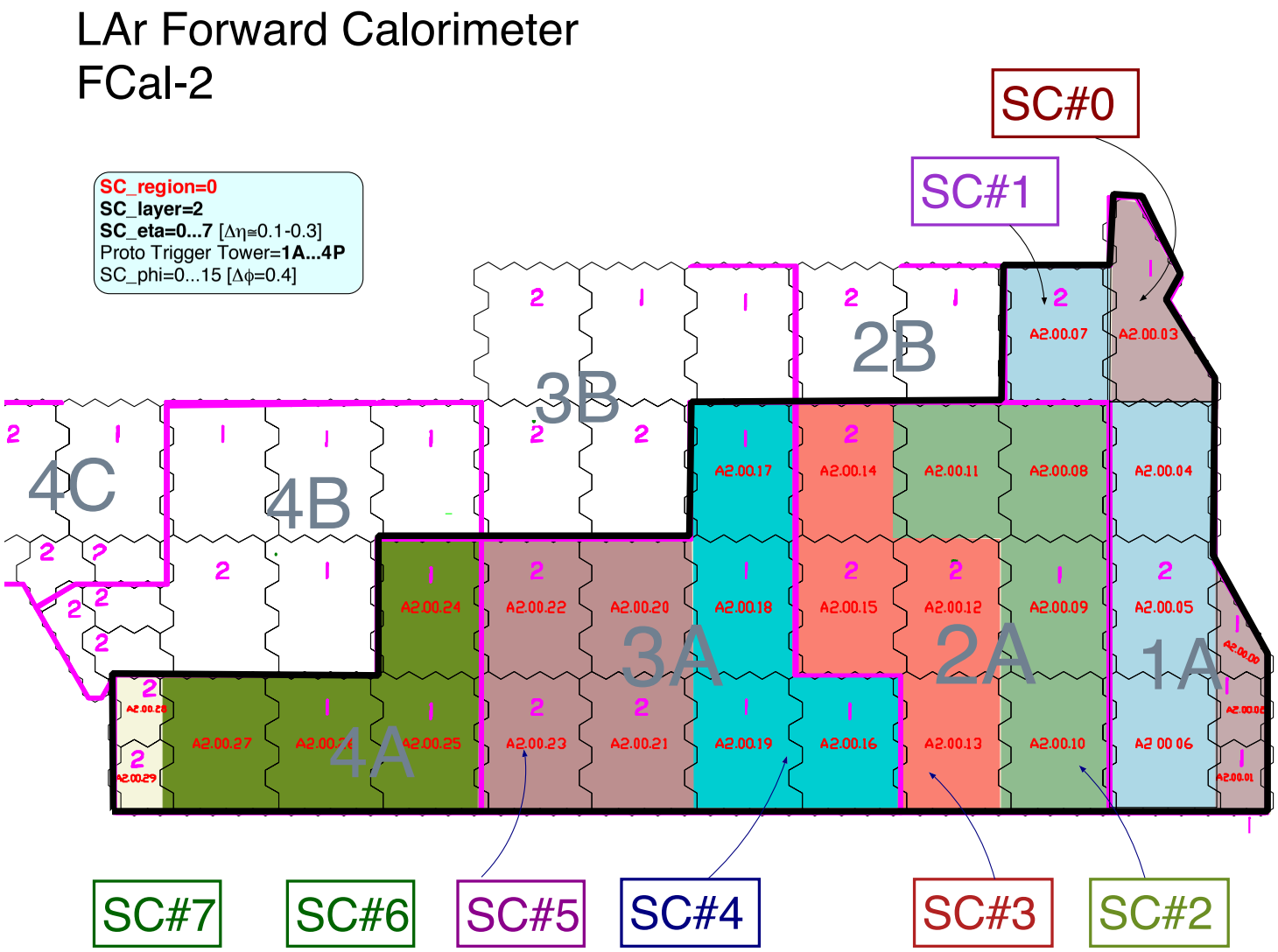

Figure 5.2. “Super-Cell” definition in theLAr forward calorimeter (FCal-2) calorimeter

LAr Forward Calorimeter
FCal-3

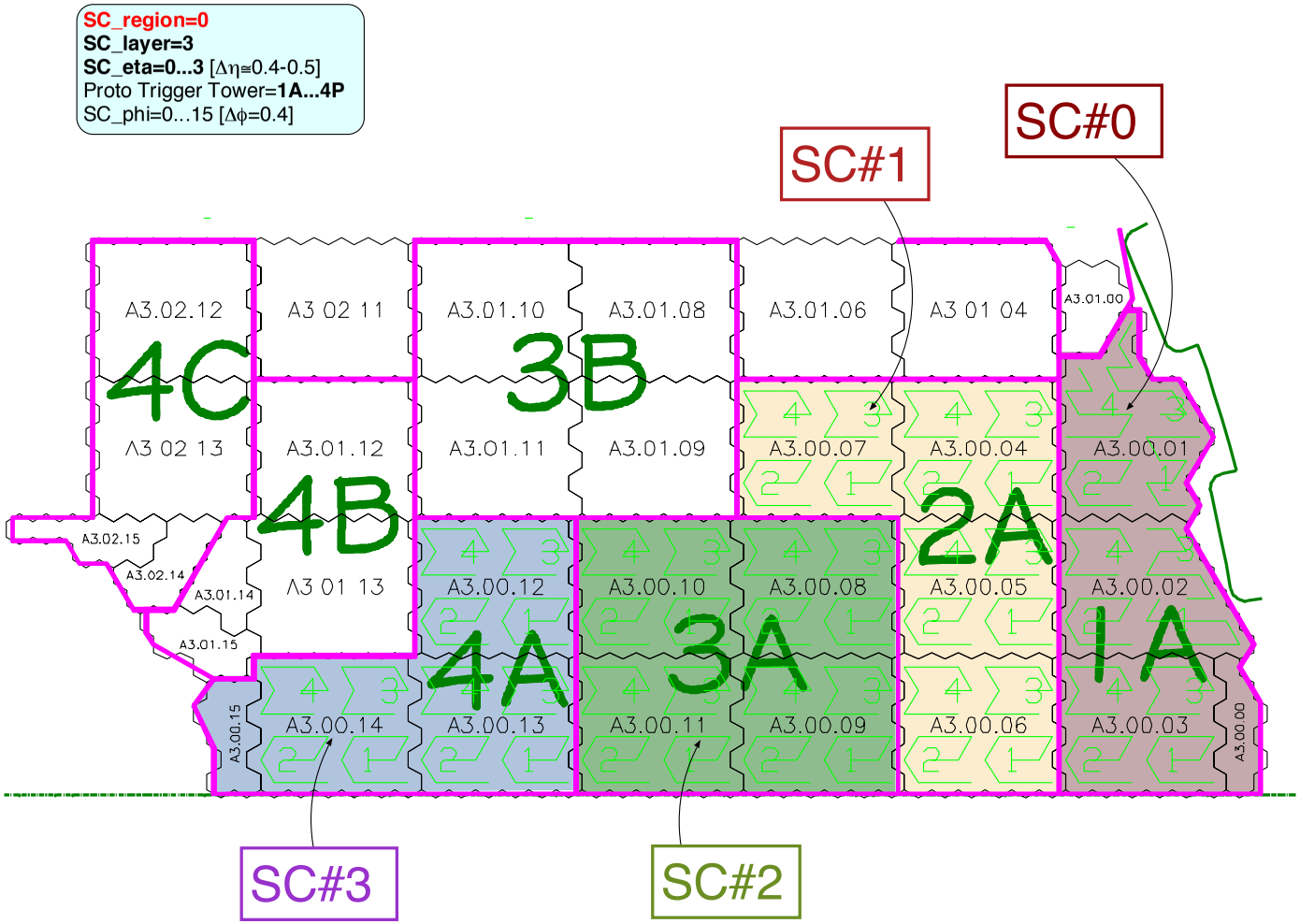

Figure 5.3. “Super-Cell” definition in theLAr forward calorimeter (FCal-3) calorimeter

6. Usage of the Tile D-layer

Dedicated D-layer outputs are available at the trigger patch panel in USA-15. The reason for this was their potential use for supporting muon identification. The value of confining the muon track to a given D-cell or via the time of flight between the D-cell and registration in the muon detector is probably marginal (2mm is needed) but needs to be studied. The advantage of using D-cell data to sharpen trigger turn-on curves has been shown to negligible (see above). Unless new contradictory results are produced it seems unlikely that the D-cells will be used to enhance the trigger.

7. Resolution and dynamic range required

The present L1Calo system receive as input EM and hadronic Trigger Towers coming from the different sections of the calorimeter after pre-summing of the analogue pulses directly in the Front-End electronics. One very important difference with respect to the cell readout, is that whilst this system has a number of gains to cover with meaningful scale the full operating range, the L1Calo system is restricted to a single gain. The noise level is the major factor to determinate the lowest significant bit of the scale and the number of bits available is a compromise between cost and the highest energy value expected for a single Trigger Tower. The minimum step used presently is 1 GeV for the EM and hadronic Trigger Towers and the saturation starts a bit before 256 GeV (8 bits). The noise level is much less than 1 GeV, particularly for the EM section and the least significant bit could be used to represent a much lower value.

For the Super-Cells, in principle, we would like to explore the possibility of using more bits as far as we can assure a similar dynamic range. It is important to remember that 4 2nd layer Super-Cells should contain 85-90% of an electron energy. Further simulations are still ongoing to verify the fraction of events which would saturate a single Super-Cell. Another important factor still not explored is the misidentification of Bunch Crossings due to pulse saturation as MC production with a correct Super-Cell pulse shape emulation is still not available. Despite these limitations, specially in the energy range of transverse energy covered by the electroweak sector, one can still provide very reasonable indications about the system to be designed.

A comparative study was made using the proposed granularity and the R_η variable implemented at the second EM calorimeter layer (ratio of energy in a 3×2 cluster by the energy in 7×2 in a cluster centered in the hottest Super-Cell). In order to explore further the flexibility of the system, we also tried a version of the same variable using only the first sample of the calorimeter. In this case, the used ratio was the energy in the 1×2 Super-Cells divided by the 3×2 Super-Cells. This is not yet certified as an interesting variable as it seems to provide information very similar to the one defined in the second layer, but it can very informative as to which energy scale one should use if further studies are to take place.

Table 7.1 presents the results with datasets at $< \mu >= 80$ ($\approx 3 \times 10^{34} cm^{-2} s^{-1}$). All variables used here were applied independently. Clearly, using 1 GeV as the least significant bit is quite damaging to the selection power of these variables. The second layer variable still keeps 58% of the jets faking electrons with this energy resolution. At 250 MeV, the gain in jet reduction for similar electron efficiency is quite similar ($> 22\%$). However, still for the second layer variable, there seems to be little gain (almost 1% of efficiency) when passing from 250 MeV to 65 MeV as the least significant bit for similar jet rejection.

For the first layer variable, however, there is a clear improvement on its selection power (0.37% in efficiency and 4.74% in rejection) when going from 250 MeV to 65 MeV resolution. This indicates that there is a level of information that can be used if the finer resolution is chosen. One possible

Table 7.1. Electron efficiency and jet survival rates for different variables and different least significant bit values. The datasets used had $< \mu >= 80$ and a preselection with L1_EM16I was used. Around 98% of electron efficiency was required.

Variable (least sig. bit)	Electron Efficiency	Jet Survival Rate
$R_\eta - 2^{nd}$ layer (1000 MeV)	98.12%	58.03%
$R_\eta - 2^{nd}$ layer (250 MeV)	97.54%	35.44%
$R_\eta - 2^{nd}$ layer (65 MeV)	98.42%	35.37%
$R_\eta - 1^{st}$ layer (1000 MeV)	98.89%	76.00%
$R_\eta - 1^{st}$ layer (250 MeV)	97.60%	46.33%
$R_\eta - 1^{st}$ layer (65 MeV)	97.97%	41.59%

explanation may lie on the fact that, given the short longitudinal size of the first layer Super-Cells ($\simeq 4.3X_o$), the energy content for the same object is much less important than at the second layer ($\simeq 16X_o$), so, the values dealt with are closer to the least significant bit values being discussed. For that reason, despite the fact that different first layer variables are still being explored, it seems reasonable to keep the flexibility provided by the 65 MeV, specially in the context of a 1-4-4-1 implementation.

Further analysis is ongoing to verify how relevant is the reduction of the least significant bit value for the hadronic layer (full trigger tower). Initial results indicate that a reduction from 1 GeV to 250 MeV would significantly sharpen the turn-on curves. For the same point of 95% of the turn on curve, this modification could potentially bring 10-20 GeV more to the 10% operating point, resulting in an important reduction on the jet rate. These results are based on inclusive, object-based, jet efficiency curves. Similar studies should be performed for event-based inclusive and multi-jet triggers, for which an overall loss efficiency on the 'plateau' is expected, and for Missing E_T triggers.

8. Front-End digitization and analog-digital interfaces

As outlined in Sec. one of the critical issues to be addressed by the C&T working group was the capability and the technical challenges of preserving the "legacy" analog information and to understand the implications and the risks in case a full digital solution was to be chosen. Also, in the case of the analog/digital option, whether the trigger tower summation and the "Super-Cell" digitization should have occurred in a single board or on separate ones. The technical challenges of the latter options were studied in particular by the LAr group for the E.M. calorimeters. Fig. 8.1 depicts a possible architecture of the front-end:

- new Layer-Sum Boards to handle higher granularity (for the first and second layer).
- The signals are driven to the new digital LTDB board, individually digitized and sent over fast optical links. The LTDB also sums the analog inputs to recreate the analog $\Delta\eta \times \Delta\phi$ 0.1×0.1 layer sums sent to the original TBB.
- For the presampler and the 3rd layer of the EM calorimeter the LSB signals are either bussed through the baseplanes to both boards, or sent to the LTDB, buffered and sent back to the TBB. These options are under study and need to be fully electrically simulated to ensure the signals characteristics are entirely preserved and for example no distortions are introduced.

For the HEC and the FCAL there is no summation on the Tower Driver board (TDB) and the board is relatively empty, therefore both digital and analog information can be integrated on a single board as shown in Fig. 8.2. Hower, the optimization of the analog signals on the baseplanes and mechanical constraints on the front-panel may suggest alternative solutions similar to the case of the E.M. calorimeters with the “legacy” TDB and a new LTDB digital only.

The feasibility study by the LAr group suggests us that the option of maintaining as much as possible the original analog signals and separate TBB and LTDB for the EM calorimeters should serve as baseline design for the Phase-I upgrades.

It is by far the less risky option considering the technical challenges on the front-end and, more importantly, the fact that the Level-1 trigger system has to be ready running from day-1 after LS2. It would introduce also flexibility in ATLAS because of the possibility of staging of the electronics to be installed off-detector.

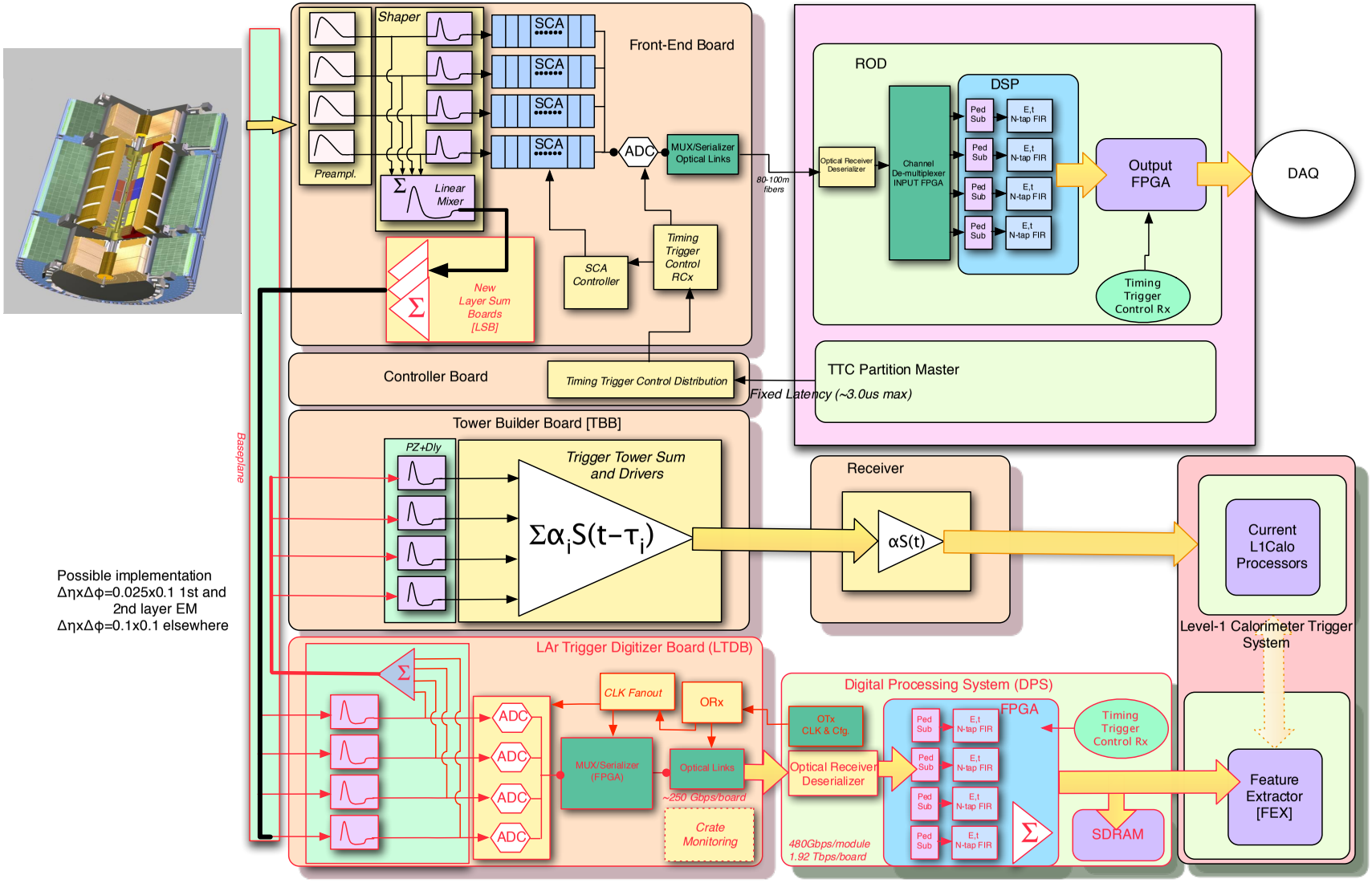

Figure 8.1. Front-end architecture with the original Trigger Tower Builder board and the LAr Trigger Digitizer Board

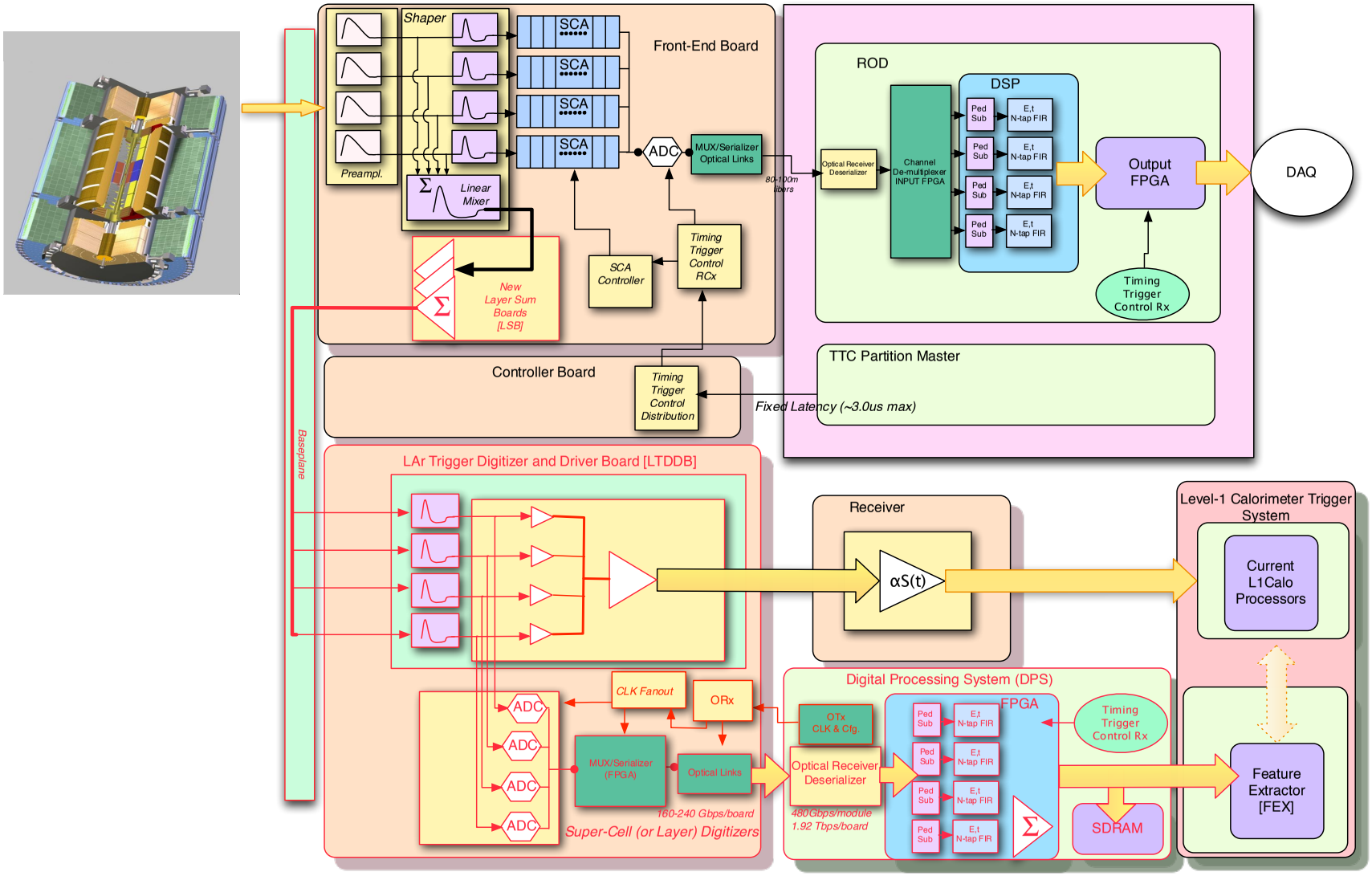

Figure 8.2. Front-end architecture with the original Trigger Tower Builder board and the LAr Trigger Digitizer Board

9. Bandwidth and organisation of optical fibers to USA15

The Front End electronics of the LAr calorimeter is directly placed on the cryostat feedtroughs with very short and well shielded connections which connect to the cables arriving from the LAr. The readout is thus repeated in “units” of feedtroughs, with two feedtroughs connected to one Front End crate. Currently, except for few special cases (End cap) the trigger sums are generated on one board for each feedthrough and sent over on twisted pair cables with differential analog signals. Normally only a change in slot placement of the TBB boards will be needed, but the hardware of boards and cables should be left unchanged.

Similarly each feedtrough electronics will have one new LTDB card. For reasons of logistics in the long cable routing, each Front End crate will be connected to the Back End system through one cable. Upon arrival at the crate, the inner ribbons of the cables will be directed to the two LTDBs on each side of the crate. The current planning calls for 4 12 fiber ribbons to connect to each LTDB. Thus an "optical cable" arriving at each Front End Crate would have 8 ribbons (plus spares). A quick estimate of the amount of data to be transferred (including some overhead for data transmission verification) implies that we need to run the links in each fiber at 5-6 GB/s. While this is a quite "conservative" link speed, a dedicated set of serializer and optical transmitters needs to be prepared which are able to operate at the radiation doses expected in the Front Crate volumes. As for the content of each ribbon, in terms of super-cells, the connectivity will be pre-sorted at the LDTB level such that super-cells in a trigger tower flow in the same fiber or ribbon, as far as possible.

The routing of the optical cables is of particular importance and since the transit times of the signals needs to be minimized for lower overall latency, the routing via the USA15-UX15 wall holes has to be used. For the same reasons, in the case of the End Cap calorimeters, the optical cables have to be placed in the Sector-9 flexible chains.

At this point more detailed work and channel counting is needed to understand the final fiber arrangement at the arrival of the LDPS. A possible option to be studied is an optical patch panel/rearrangment box placed in the USA15 racks which regroups fibers/ribbons from different origins and reorders them such that the flow through the FPGA’s in the the LDPBs, assuming a 1-to-1 transparent input-output, is optimized for the further connection to the LVL1 FEX system.

10. Architecture of the LDPS

The LAr Digital Processing System (LDPS) is receiving the “Super-Cells” information and preparing it to to pass on to the FEX processors. Hardware wise the system is made of FPGA based DSP "calculators" which are housed on LAr Digital Processing Blades (LDPBs) which on their turn are placed in crates (or ATCA Shelves in the current system choice). These crates are located in the USA15 racks close to the current LAr Trigger Receiver and L1Calo Pre-Processor and Processor systems, this is the first row (closest to the UX15-USA15 wall) on USA15-Level 2 plant. Sufficient rack space (not currently used) has been identified in this row.

Following the path of the data illustrates the functions of the LDPS. The fibers arriving from UX15 into USA15 bring the 40 MHz digitized samples of each supercell. A certain number of super cells (up to $\sim$25 [i.e. 320/12])12-bit words of digitized samples arrive serially in each fiber. As already mentioned, if necessary, they might be rearranged and regrouped into fiber ribbons covering 0.1×0.1 towers. The optical signals are connected trough transducers to the inputs of FPGAs. The input connectors/transducers, FPGAs and output transducers/connectors are placed on mezzanine boards of a LPDB (see Fig. 10.1). The current plan is to place four of these mezzanines on each ATCA blade slot. This density is mainly driven by the real state for optical connectors on the

front panels or PCB surface and detailed design/prototyping has yet to be started. The total count of channels needed would be housed possibly in 3 or 4 ATCA shelves. The LDPB motherboard covers other functions of the ATCA system like power control, in-board and board-to-board system communication.

The algorithms implemented in the FPGA include a 40MHz bunch-by-bunch energy calculation and bunch crossing identification for each supercell. The output information is synchronous to the LHC 40 MHz clock with a fixed latency. To perform this calculation, calibration and geometrical constants for each channel are pre-placed in the FPGA memories. An algorithm, e.g. a linear sum like Optimal Filtering or other is applied to the 40 MHz samples and the output as GeV calibrated transverse energy is sent to the eFEX system. The number of bits and LSB value of this energy still need to be understood. Additionally energy sums have to be calculated adding supercells to 0.1×0.1 towers which are transmitted to the jFEX system. Other more global information (larger area sums or vector component sums) might also be calculated and passed on to the jFEX.

Additionally to the synchronous information, more global calculations may be performed at the LDPB level, combining information available from all super cells connected to the board. The ATCA fabric connections (e.g.10Gb ethernet) can be used to collect all this data as well as channel calculation monitoring information in a central slot and passed on to a readout system for monitoring purposes or further contribution in the upper-level trigger system (e.g. LVL2).

LDP System-LDP Board Scheme

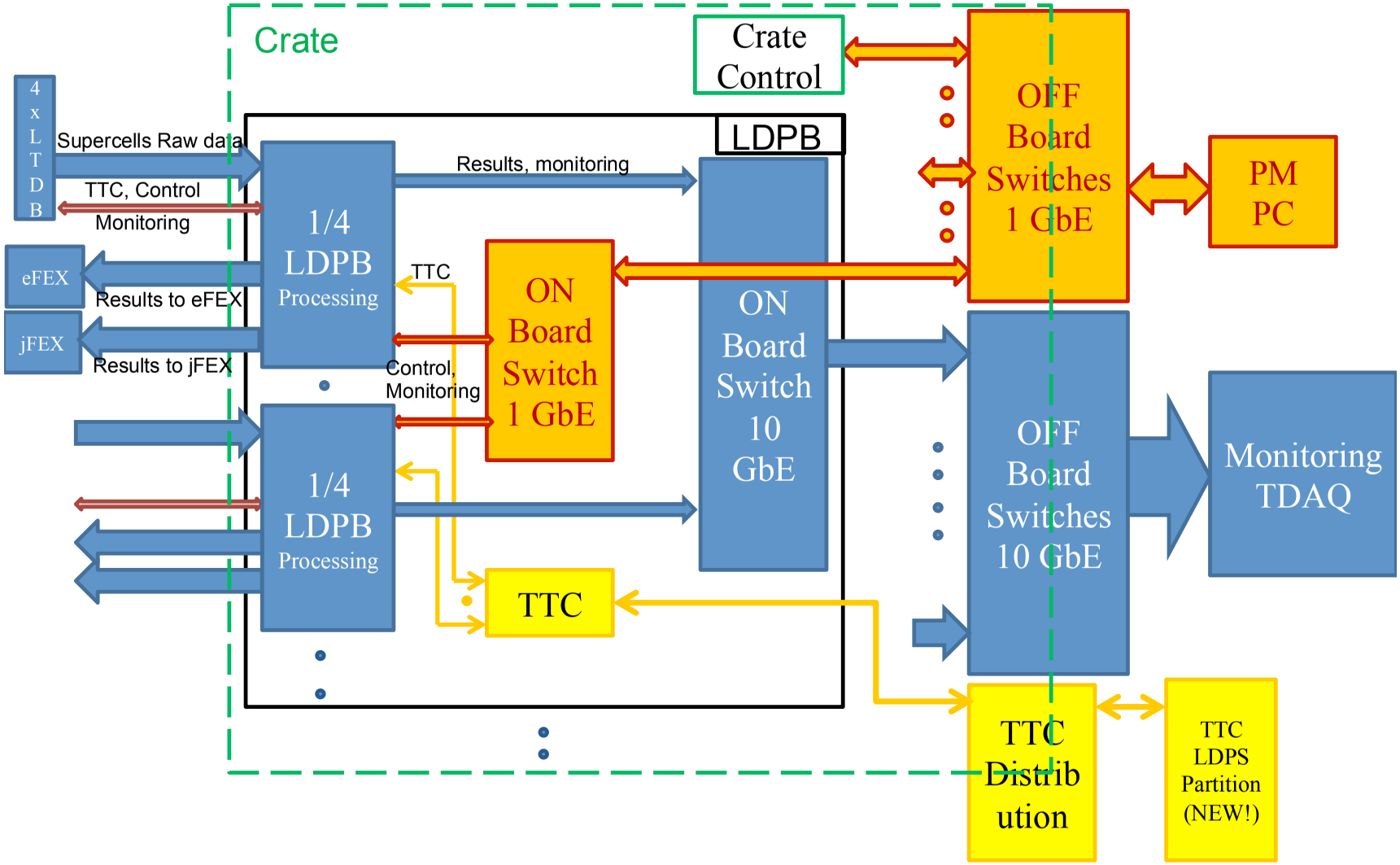

Figure 10.1. BLock diagram of the LAr Digital Processing board.

11. Bandwidth and organization of optical fibers from DPS to FEX

The DPS output to the two FEX subsystems will be distributed optically at multi-Gbit data rates by a large fiber plant. The links are assumed to be fixed-latency and synchronous to the LHC machine clock, and the content and organization are dependent on the link speed and protocol chosen.

For the purposes of this report a conservative link speed of 6.4 Gbit/s is assumed, or 160 times the LHC bunch clock rate. We also assume an 8b/10b data protocol for the links, which has the lowest protocol overhead. With these assumptions, each optical fiber can deliver a data "payload" of 128 bits per LHC bunch crossing.

Research and development projects are underway to determine (among other questions) whether link rates higher than 6.4 Gbit/s may be reliably implemented in a large distributed system. If so, the constraints outlined below may be significantly relaxed.

For E.M. layer distribution to the eFEX, time-multiplexing of supercell pairs in consecutive bunch crossings (a scheme commonly referred to as BCMux) is strongly favored by the L1Calo collaboration, since it allows the largest portion of the fiber plant to be essentially halved. The following sections assume that BCMux is used.

11.1 E.M. data to eFEX

Assuming the 1-4-4-1 supercell arrangement and s, a typical E.M. tower will include ten supercell sums. Using BCMux, two adjacent E.M. towers can be transmitted over a single 6.4 Gbit/s fiber link, with a dynamic range of up to 11 bits per supercell. The BCMux scheme adds an extra protocol bit to each supercell pair, so the total data payload per BC becomes (11+1)*10, or 120 bits per BC. The extra eight bits may be used for checksums or other purposes.

11.2 E.M. data to jFEX

The jFEX is currently assumed to receive 0.1×0.1 granularity tower sums produced by the DPS. Because they are summed from up to ten supercells each, tower sums may be non-zero in consecutive BCs, so BCMux cannot be used to reduce the jFEX output volume.

Each fiber link to jFEX can easily accommodate a group of eight E.M. towers with dynamic range up to 14-15 bits, with bandwidth remaining for

11.3 Fiber duplication and routing

As described in followings section, the eFEX and jFEX will typically require two copies of each fiber link. The favored solution is to perform this at the outputs of the DPS, using four sets of parallel-optic transmitters (two to eFEX, two to JFEX)

An "Optical Patch Panel" network will receive the 12-parallel ribbon fibers from the DPS, rebundle and distribute them to the eFEX and jFEX in 48-fiber bundles with MTP/MPO headers.

Due to technical challenges in eFEX partitioning, some links to that subsystem may need four-times duplication. The details of this are open at this time.

12. Architecture of the Level-1 Calorimeter Trigger system in Phase-I. Routing of the legacy analogue signals and of the digital “Super-Cells”

Two separate feature extractor subsystems are planned for Phase-1 to take advantage of the digital readout from the E.M. calorimeters. The e/γ feature extractor (or eFEX) will work at supercell granularity, identifying isolate electromagnetic and hadronic clusters in overlapping, sliding windows of size up to 0.5×0.5 in $\eta\times\phi$. The jet feature extractor (or jFEX) is currently foreseen to

receive 0.1$\times$0.1 tower sums from both the E.M. and hadronic layers to identify jet candidates in sliding windows up to at least 0.9$\times$0.9.

12.1 FEX architectures

The eFEX and jFEX subsystems will have very similar architectures, and use many of the same design elements.

Both are planned as modular subsystems, installed in ATCA shelves. Input data from the E.M. and hadronic layers are routed optically from the back of the crate and through Zone-3 to 12-channel, parallel-optic receivers on the main processing boards. The converted signals are then distributed to large FPGAs that perform the feature extraction algorithms, transmit the real-time results optically to the L1Topo processor, and read out L1A accepted events to DAQ and Level-2.

To provide the necessary angular coverage to implement overlapping sliding-window algorithms, the input links received by each processor FPGAs must include duplicates of those received by the âĂŸneighboringâĂŹ FPGAs in Îů and ÏĘ. For link sharing between FPGAs on the same board, electrical duplication is foreseen, using a loopback feature of the FPGA transceivers. Sharing between boards is achieved by link duplication at the source (i.e. the DPS output).

12.2 Hardware Constraints on eFEX and jFEX partitioning

Partitioning of the two FEX subsystem is constrained primarily by currently available optical links and connectors, FPGAs and the ATCA form factor. Board complexity and power considerations may cause further restrictions.

The baseline assumption for optical link speed from the DPS to the FEX subsystems is 6.4 Gbit/s, or 160 times the LHC bunch clock. Higher link speeds may well be achievable in a large, distributed system, and are under investigation. The baseline choice of optical transmitter/receiver is Avago MiniPod, a 12-fiber parallel-optic device with small footprint and high light intensity.

Ribbon fibers are fanned out to the MiniPods on the main FEX modules by âĂIJoctopus cablesâĂİ from the optical feed-through connectors in Zone-3. Each feed-through can contain up to 48 fibers, and the Zone-3 connector height allows up to four feed-throughs per module. This sets a practical limit of 192 fiber input links per FEX module, or 16 MiniPod receivers.

For the processor FPGAs themselves, the most important constraint is the number of available multi-Gbit transceivers. The Xilinx Virtex-7 family includes mid-range devices with large amounts of logic resources and up to 80 transceivers each. Taking into account the requirement to receive duplicate links from neighboring FPGAs, this sets a practical upper limit (for the eFEX) of around 64 fiber links to a single FPGA, a third of the maximum fiber budget per module. Since this leaves no spare input links for other functions, a more realistic scenario is a maximum of four FPGAs per module, with an average of up to 48 input fiber links per FPGA.

12.3 Routing of digital EM supercells to FEX systems

The eFEX receives up to ten supercell sums per E.M. tower. Assuming the use of bunch-crossing multiplexing (BCMUX), this allows all supercell sums from two neighboring E.M. towers to be transmitted using a single 6.4 Gbit/s fiber link. By comparison, the jFEX receives a single digital sum of all supercells in each EM tower. This, prevents the use of BCMUX to reduce link count, but the smaller data volume per tower allows one 6.4 Gbit/s fiber link to transmit a group of at least eight E.M. towers.

As mentioned above, the DPS should provide duplicate links to neighboring FEX modules to allow seamless overlapping window algorithms. By choosing an eFEX geometry where each processor module covers a partition in η or ϕ that is at least 0.4 wide, two copies of each link are

sufficient in most or all cases. Similarly, jFEX module geometries covering partitions at least 0.8 wide in η or ϕ would also typically require just two copies of each optical link.

Due to link and board density issues, such a mapping may be unfeasible. One proposed eFEX partitioning scheme divides the system into two ATCA shelves, with each processor module covering a region roughly 0.4 in η and 3.2 in ϕ. This would require four-times duplication of links near the $\phi = 0, \pi$ boundaries.

12.4 Routing of legacy analog hadronic towers to FEX systems

12.4.1 Datapath through the nMCM

For Phase-1, the hadronic layer is still brought to L1Calo as single-tower, analog transverse-energy sums. It is proposed to augment the L1Calo real time data path to extract copies of the hadronic tower sums and transmit them in digital form to the eFEX and jFEX.

Work is already underway over the 2013-14 shutdown to upgrade the L1Calo PreProcessor with new, FPGA-based multi-chip modules (nMCM). Among other benefits, these nMCMs can be configured to serially transmit the 0.1ÃŮ0.1 hadronic tower sums to the Jet/Energy-sum processor subsystem (JEP), instead of the presumed 0.2$\times$0.2 âĂŸJet elementsâĂŹ currently sent.

The Jet/Energy-sum modules (JEMs) in the JEP crates each receive serialized data from the PreProcessor on four FPGA-based daughter cards. These daughter cards will be upgraded to receive and process the finer-resolution data. Jet-element sums with 0.2ÃŮ0.2 granularity will be formed and distributed to the legacy jet algorithm while the full-granularity tower information will be transmitted serially to an upgraded. optical link daughter card on each JEM that will send copies of the hadronic layer to the eFEX and jFEX (see Fig. 12.1).

The fanout considerations in the previous subsection apply equally to the hadronic information. In general, the eFEX and jFEX should each require two copies of each input link. But challenges in partitioning the eFEX may require some links to be duplicated four times.

12.4.2 Datapath through a TileCal Trigger Digitizer Board in USA-15

Alternatively, for the improvement of the TileCal trigger tower resolution and possibly some improvement on the TileCal trigger tower signal to noise ratio, a TileCal Trigger Digitizer Board (TTDB) could be designed and placed at USA15 cavern (see Fig. 12.2). This board should digitize both TileCal trigger tower and D-Layer signals with a 12 bit ADCs, keeping an analog path to the current level one, and transmit the data through optical links up to the new âĂIJsuperâĂİ Read Out Drivers (sROD). The sROD should perform the energy estimation of the TileCal trigger signals and communicate with the FEX processors. Additionally, the development of the TTDB could be in consonance with the TileCal front-end and back-end electronics upgrade program, as it could use similar boards, systems (Daughter Board and sROD) and components (12 bit ADC from Main Board). Therefore, several boards and components of the new TileCal front-end and back-end electronics could be tested in ATLAS during Phase-I.

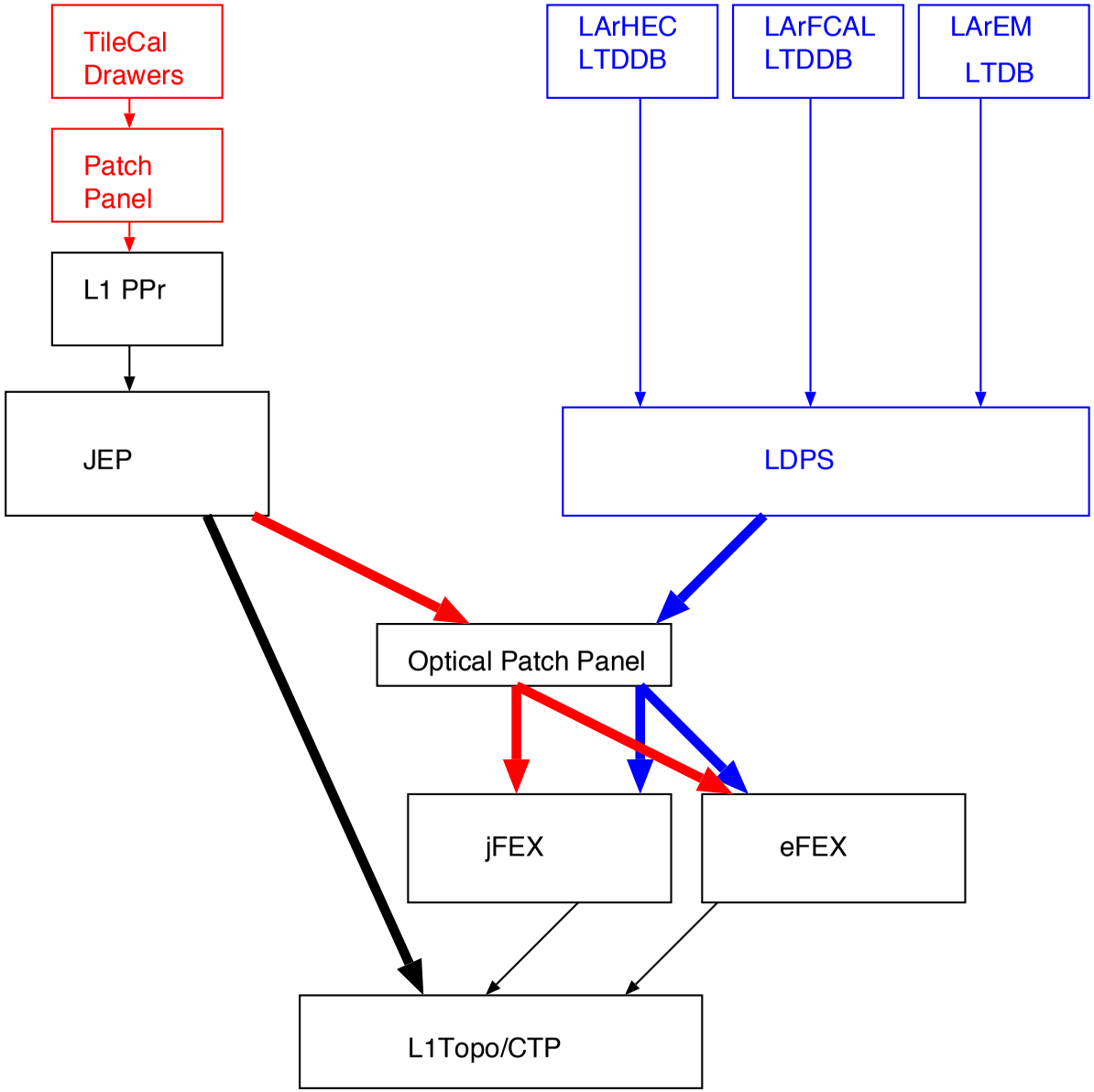

Figure 12.1. Possible datapath of the “legacy” TileCal trigger tower through the MCM/JEP modules.

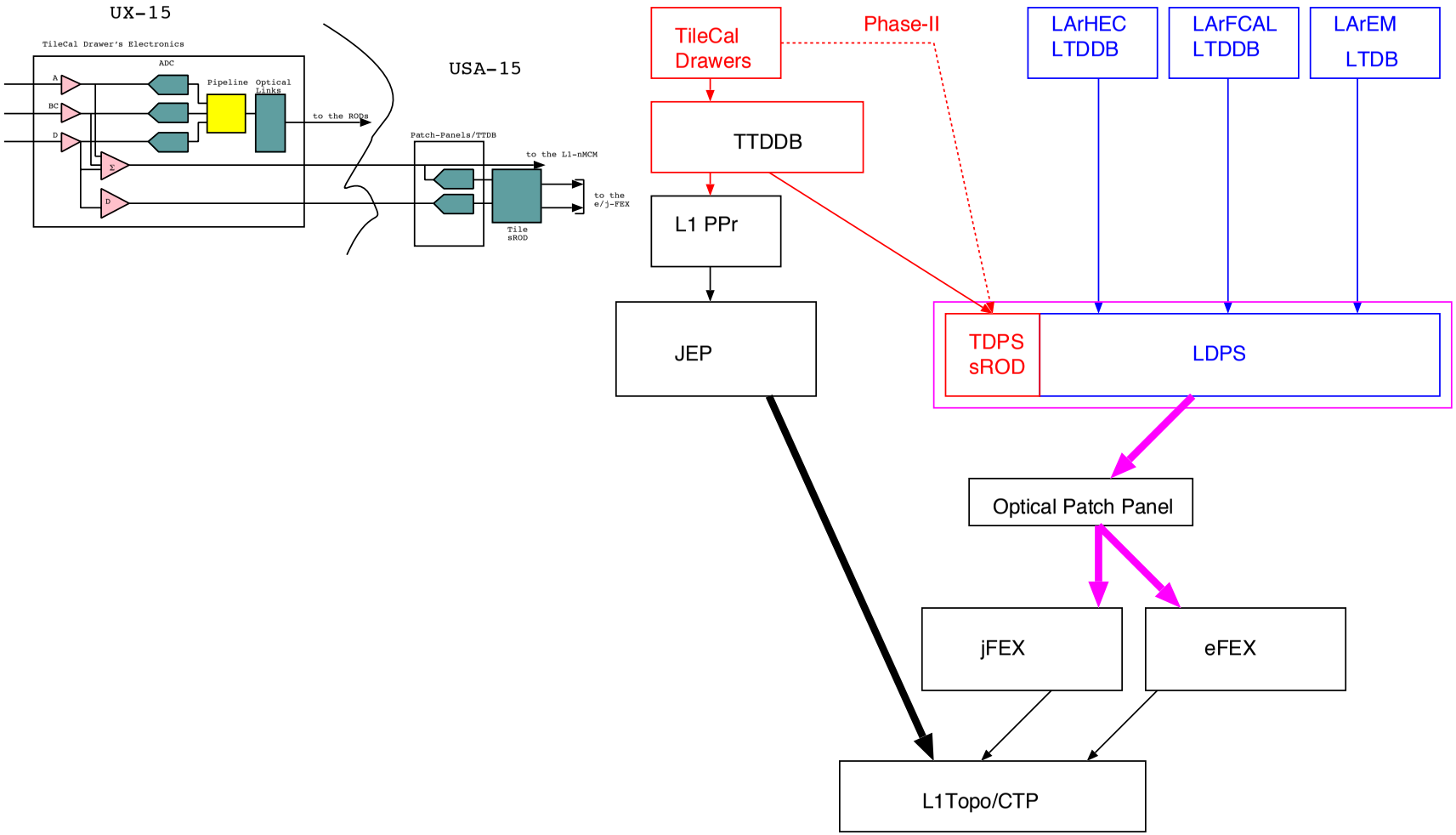

Figure 12.2. Possible datapath of the "legacy" TileCal trigger tower through a TTDB in USA-15 patch-panel crates.

13. Latency

Latency estimates for the architecture described in Secs. 8, 12 have been made previously by the Phase-I Upgrade Sub-committee (Ref. [4]) and updated since to take into account for example a better understanding of the front-end digitization steps, and the evaluation of the serialization/deserialization stages at each interface (Ref. [5]).

Figs. 13.1 and 13.2 represents schematically the latency budgets for the different components of the existing system and for the proposed system in Phase-I. Currently, the output of the CTP the latency is 76 BCs. The downlink to the system front-ends has been implemented differently:

- For LAr the L1A is sent through the TTC fibers passing in the trigger hole (70m = 14BCs) to the Front-End board. The decoding of the trigger signals in the TTCRx is estimated to be 4 BCs increasing the delay by approximately 18 BCs for a total of 94 BCs. The constraints for the LAr system derives from the fact that the analog pipelines (144 cells) are also used as derandomizing buffers, so an increase in latency potentially introduces dead time. However, if required the dead-time increase may be compensated by the reduction in number of samples to read out, which drastically reduces the number of events that can be stored temporarily in the derandomizing buffers. This is being already planned for the 14 TeV run in 2014 to be able to increase the trigger rate to 100kHz.

- In the SCT the TTC signals are rounted through the RODs and down through the normal readout path (110m=22 BCs). The total delay at the front-end is estimated to be 102 BCs. There are 18 reserved addresses in the SCT front-end ASIC's digital pipelines. (DON'T UNDERSTAND)

- A L1Topo processor is installed in LS1. It introduces a latency of approximately 8 BCs, to which an additional 1.5 BCs for the CTP has to be included. Furthermore, the new muon trigger logic from the new small wheel will add about 3 BCs. The CTP output L1 latency is therefore 88 BCs and the delay to the front-end will increase to 114 BCs (see Fig. 13.2

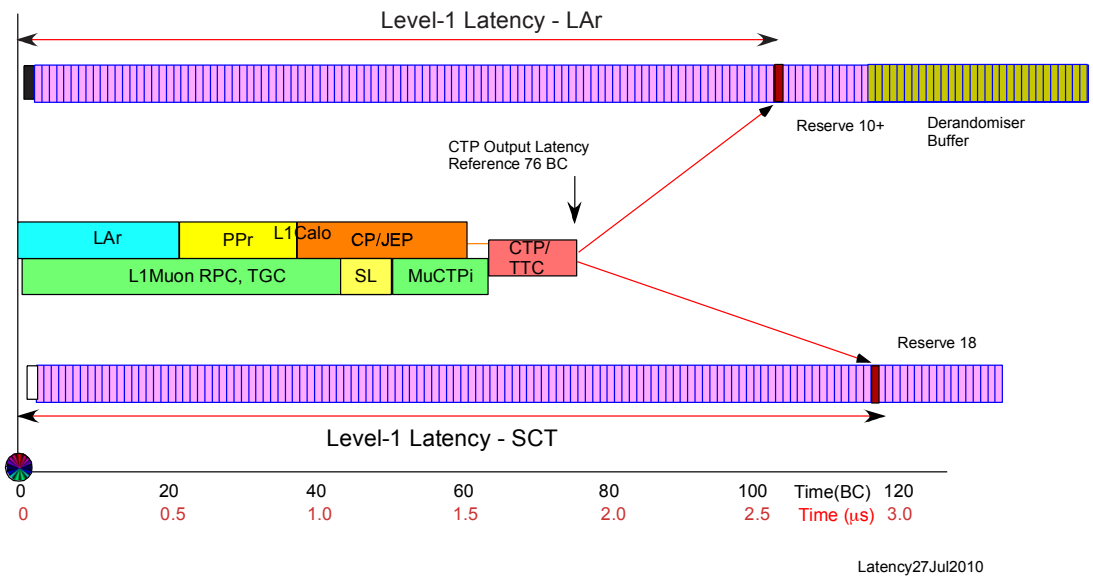

Figure 13.1. Latency budget of the existing L1Calo trigger for the Phase-I upgrades.The output of the CTP is estimated to provide a max. latency of 76 BCs.

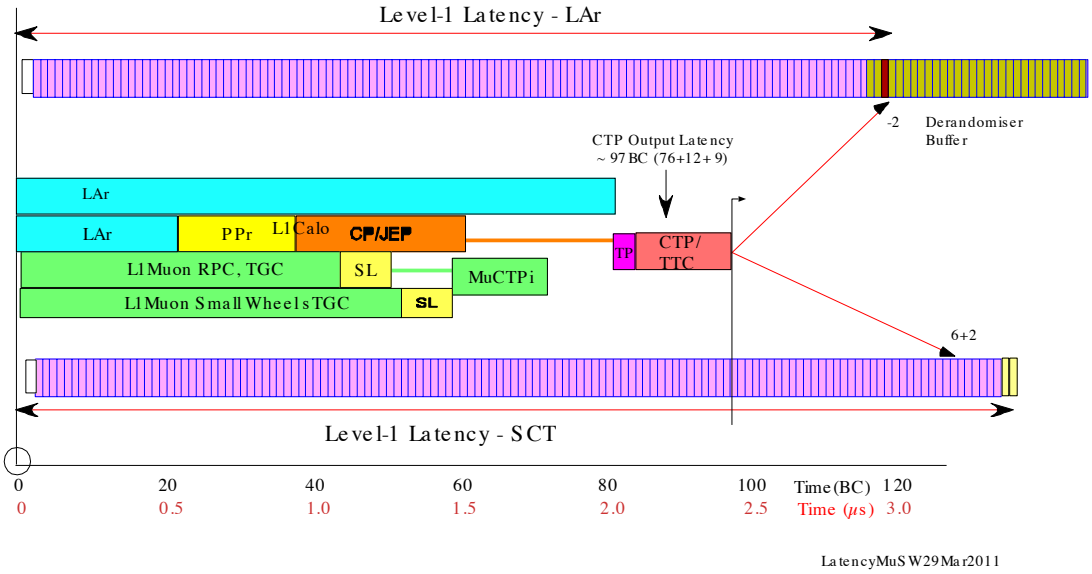

Figure 13.2. Latency budget of the planned L1Calo trigger for the Phase-I upgrades. The L1Topo and the new L1 MuCTPi trigger logic will increase the latency at the output of the CTP by 12 BCs. The addition of the L1Calo system processing the high granularity information from the calorimeters will increase the latency by other 9 BCs approximately

A conservative estimate of the additional latency required in Phase-I with the upgrades of the calorimeter trigger interface, increases the latency the CTP input signal by approximately 6-8 BCs. The main uncertainties on the budget estimates is due to ADC's digitization times, and by the serializer/deserializer operations in the ASICs, optical links and receiving FPGAs. Fig. 13.3 summarizes in a few tables the details of the latency calculations for each subsystem.

LAr + L1Calo

	BCs	Sub Total	Total
LAR Analog (TTB+Receivers)			
Time-of-flight to endcap at eta = 2	0.6		
Cable to pulse preamplifier	1.2		
Pulse preamplifier and shaper	0.4		
		2.2	2.2
Pulse peaking time	2		
Cable to tower-summation board	0.2		
Analog summation	0.4		
Cable to USA15 (70 m)	14		
Receiver station			
Cable via patch panel and PPM	3.4		
		20	22.2
L1Processors			
In parallel w. jet/Et finding: PPM (preprocessor for e/gamma, tau/hadror	14		
LVDS Cable to CPM (11m)	2.2		
CPM (cluster processor module)	13.5		
CMX (updated CP CMM, excluding serializers	8		
		37.7	
In parallel w. e/g, t/h: PPM (preprocessor for jet, Et)	15.5		
LVDS Cable to JEMs (11m)	2.2		
JEM (jet Et processor module)	7.5		
CMX (updated J/E CMM, excluding serializers	9		
		34.2	59.9
Cable to CTP (11m) for trigger sums	2.2		
CMX Output Serializers	2		
Optical Fibers to L1Topo (11m)	2.2		
		4.2	64.1

LAR System Upgrade Scenario 1 (L1 only)

	BCs	Sub Total	Total
LAR Analog + Digital (LTDB+DPS)			
Time-of-flight to endcap at eta = 2	0.6		
Cable to pulse preamplifier	1.2		
Pulse preamplifier and shaper	0.4		
		2.2	2.2
Pulse peaking time	0		
Digitization on LTDB	7		
Multiplexing on LTDB	1		
Serializer on LTDB	2		
Optical cable (70 m) from LTDB to DPS	14		
		24	26.2
Deserializer on DPS	2		
Channel demultiplexing on DPS	1		
Pedestal subtraction	1		
E, t, Q, N-tap FIR, BCID	5		
Digitial summation	2		
Multiplexing on DPS	1		
Serializer on DPS	2		
Optical cable (15 m) from DPS to FEX	3		
		17	43.2
FEX			
Deserializer on FEX	2		45.2
Data duplication between FPGAs	0.5		45.7
Channel demultiplexing/synchronization	1		46.7
Primitive processing (e/gamma, tau/hadron, jet, E	5		51.7
Multiplexing	1		52.7
Serializer	2		54.7
Optical cable (10m) to L1Topo	2		56.7
		13.5	56.7

	BCs	Sub Total	Total
L1Topo			
L1Topo Input Deserializers	2		
Synchronize to local clock	0.5		
Algorithmic Processing	1		
		3.5	
Electrical Output to CTP	0.5		
Eectrical Cable to CTP (2m)	0.4		
		0.9	
Output Serializers for optics (if used)	2		
Fibrest to CTP (if used) (2m)	0.4		
		2.4	
		5.9	70
CTP			
CTP Input Delay		**2.6**	**72.6**
Last Electrical Signal arrival			
CTP_In processing + PITbus	3		
Last Input Data available for processing			
New CTP_CORE: processing and outpu	2		
CTP Out	2.5		
Cable to LTPi (10m)	2		
LTPi+LTP+TTCvi+TTCex	2		
Variable Delay	2		
		13.5	**86.1**
Fibers to FE electronics (110m)	22		
TTC Receiver	4		
		26	**112.1**
TOTAL			**112.1**

Figure 13.3. Detailed estimates of the L1 latency budget in Phase-I

14. Compatibility with Phase-II

The architecture proposed seems consistent with the currently proposed plans for the upgrade of the trigger system in Phase-II, despite the fact that they are at an early stage. However, for TileCal this means that the completely new electronics (on and off-detector) will feed the e-FEX and j-FEX directly replacing the intermediary solution chosen in Phase-I. Maybe some of the components (early sRODs) could be re-used but this is not certain, since their technology would be about 4 years older than the new components. In case of a dual hardware-based first level trigger (i.e. L0/L1) the system under consideration would naturally mature into the future Level-0. If ATLAS, instead will decide to have a single Level-1 trigger with an extended latency and rates up to, letâĂŹs say, 500kHz, still the LAr part of the system installed in Phase-I could constitute the core of the input stage of the clustering, e/g and jet/E processors, with the possibility to access even higher granularity information from the calorimeter RODs to improve selectivity (but obviously this scenario has to be fully investigated).

15. Conclusions

We have reviewed different scenarios for the upgrade in Phase-I of the calorimeter trigger at Level-1. A summary of the finding, the main recommendations have been summarized in Sec. **??**. The most important open questions, which will need to be addressed either by the time of the ATLAS upgrade project approval or in any case for the preparation of the Technical Design Report are also listed. The management of the LAr, TileCal and TDAQ systems involved have suggested that, after its conclusions, the WG would be maintained alive as a forum of discussion to define and decide over the technical details still open. In this case, Sec. is meant to summarize what the priorities to be addressed in the next 3-6 months are.

References

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[3] H. Chen et al., *Proposed mapping and definitions of the Trigger 2 Super-Cells for the Phase-I Upgrade LAr*, Note in preparation, 2011

[4] C. Bohm, et al., *Report of the Phase-I Sub-Committee*, EDMS Document No. 1155027 (ATU-ORG-MR-0001) https://edms.cern.ch/document/1155027/1, 2011

[5] N. Gee, *Level-1 Latency update, Phase-0 & I*, https://indico.cern.ch/getFile.py/access?contribId=6&sessionId=0&resId=1&materialId=slides&confId=190420, Mini-TDAQ week - July 2012.