FPGA XC7K160T - 676 balls

Two packages available, same footprint:

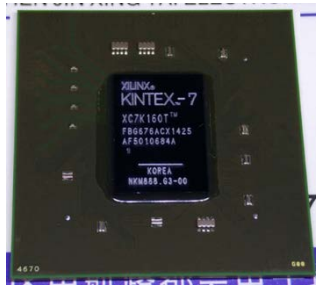
FBG vs. FFG, slightly different supply decoupling and VccAuxIO use

Cost vs. I/O speed (6.6/12.5Gb/s) (~25% in cost ?)

Thermal properties 8.9 vs.7.5 °C/W. heat sink type ?

Suggestion: try to make power distribution system compatible to both packages and decide later

- What type has been on the first iteration **?**
- Anybody available to double check compatibility**?**



Design changes:

- Add MGT uplinks to future MARS replacement

→ Require separate supply voltages / regulators (1V, 1.2V, 1.8V)

→ Need to choose suitable cable type/socket (see below)

- 4 FPGAs → 3 FPGAs : redistribute I/O lines

→ Decision on use of High Range and High Performance I/O
HR: 2.5V, **no output delay tuning**, HP: 1.8V, all LVDS

- HR and HP have different I/O delays (mixed in design ?)
- Single ended / DCI ?

Further mods

Operation in mag field

- Linear regulators only on active daughter
- Requires separate at least two external supplies of ~1.2-1.5V and ~4V to keep dissipation down.
- Exact grouping depends on power requirements per individual voltage node (1.0, 1.2, 1.8, 2.5, 3.3 … ???)
- Extend MARS interconnect with cable links :
  length vs. bitrate. Example : Current ATLAS L1Calo PPM to jFEX links: > 10m @ 480Mb/s per pair (with passive pre-compensation and high-end cable)
- Future iteration: Use small number of MGT links (up to 6.6 (or 12.5) Gb/s) built-in equalizer, length vs. bitrate ???????
- Aim at industry standard connection → correlation between cable and socket type. RJ45/USB3.0/3.1/SATA/…

Firmware mods:

In Apr. 2017 there seemed to be quite a lot of flexibility on Jiri K's end, not quite so @ HH… will need kind of review ?!?!