CALICE / Silicon PM activities

Detector and readout electronics development

- Development of a system for mass production of AHCAL "HBU" scintillator/PCB sandwich
  - P. Chau
- Data aggregator and timing unit for CALICE / AHCAL
  - A. Welker, R. Spreckels, J. Caudron
- Optimization of scintillator tile geometries for surface mount (digital) SiPMs
  - Y. Liu
- Generic Silicon PM R&D
  - S. Krause

Technical Support :

B. Bauss, R. Degele, K.-H. Geib

Supervision:

V. Büscher, L. Masetti, U. Schäfer, S. Tapprogge, R. Wanke

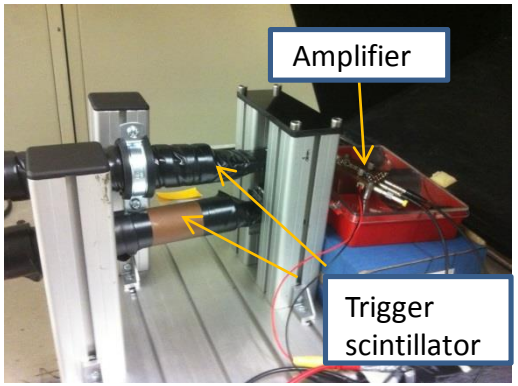
Mass Assembly of AHCAL

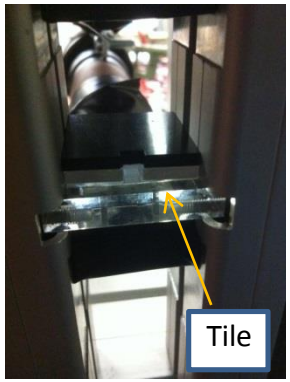
Motivation:

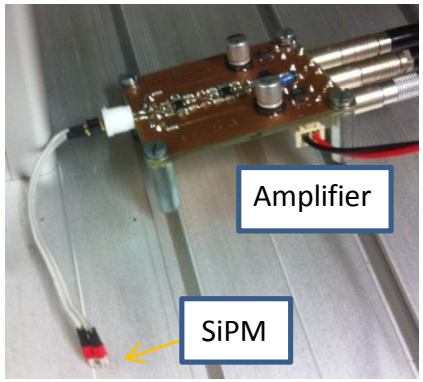
- About 8.000.000 tile scintillators have to be placed on boards
  → Automatic assembly is needed

Status:

- Procedure for fast mass assembly has been defined
  → Mass assembly requires numerous design modifications
- Tests of modified tile design (optical properties) are running with cosmic rays







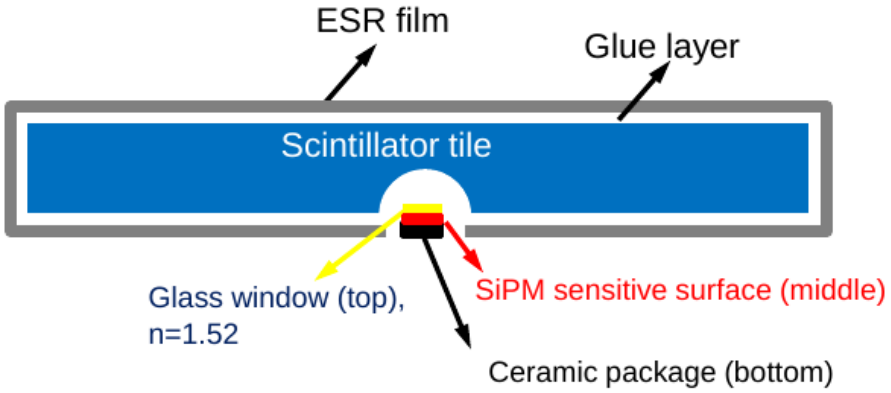
→ First results: Better/similar properties than with current design

- Camera tests (for tile detection) are successful
- HBU board design changes for automatic soldering process are defined

Outlook:

- Temperature tests, optimization of modified tile design
- Functionality tests for assembled boards

Study of scintillator tiles geometry using Surface Mounted SiPM

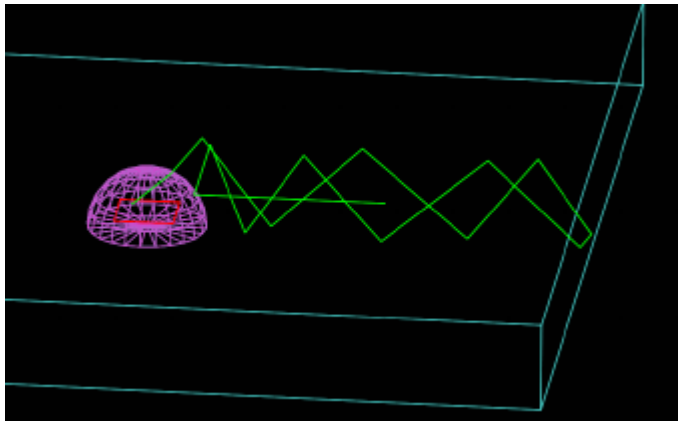


Motivation:

- Surface mounted SiPM are easier to solder on HBU board automatically
- SiPM can be placed at the centre of the tile → Better uniformity

Status:

- Exploration of a large quantity of scenarios:
  - Geometry, optical surface, reflectivity of the wrapping, …
- Based on simulation (Geant4) with consistent modelling (PDE, Scintillator Emission Spectra, …)
- Computing power required
- Comparison with Data recorded in Aug 2013 by MPI Physik, Munich

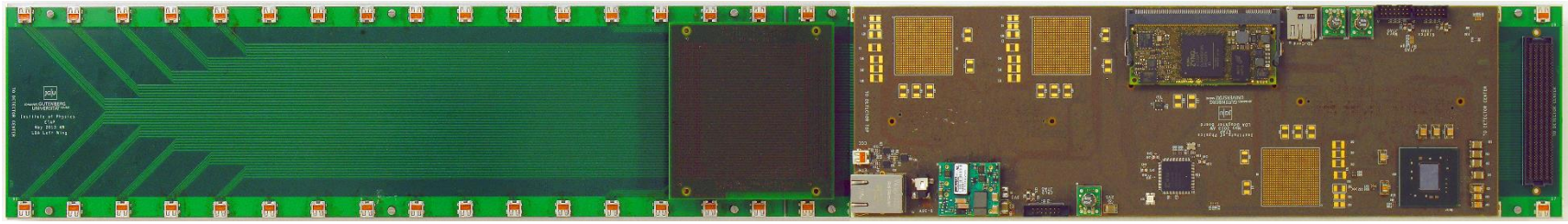


Outlook:

- Few scenarios have been ruled out
- Some parameters seem promising
- Comparison with Data on-going
- Development of more realistic modelling

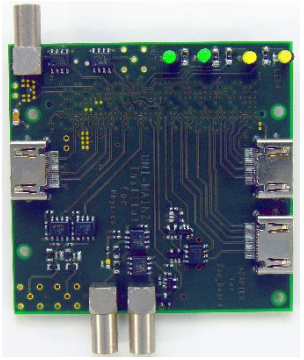
<<< Activities throughout 2013/14 >>>

AHCAL wing LDA and CCC



Development of a data aggregator for the "Analogue" HCAL of CALICE

- Consolidation of data received from the HBU active detector units (~ millions of channels)
- FPGA and Xilinx Zynq based
- Data transmission into DAQ via Ethernet
- PCB geometries adapted to final detector geometry
- → 1.1m long structure consisting of central body and two wings
- Status
  - Initial prototype successfully built
  - Firmware work, software integration and tests on-going



Development of a timing unit for CALICE

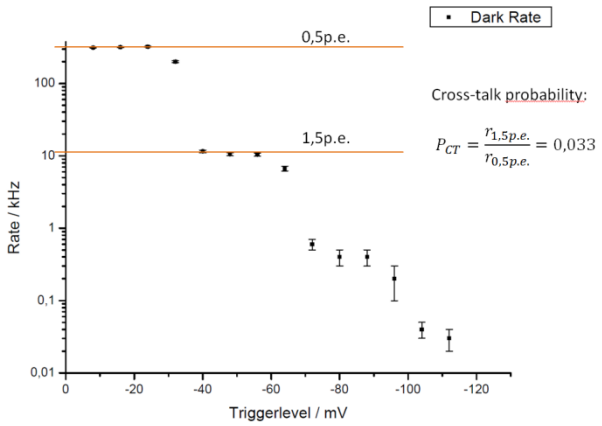
- Distribution of central clock
- Synchronous commands to all sub-detectors
- Busy handling, asynchronous trigger (for beam tests)
- Status
  - Successful operation in ECAL beam tests
  - Initial version made available to AHCAL collaboration

+ Development of various test and support modules (FPGA/Zynq based)

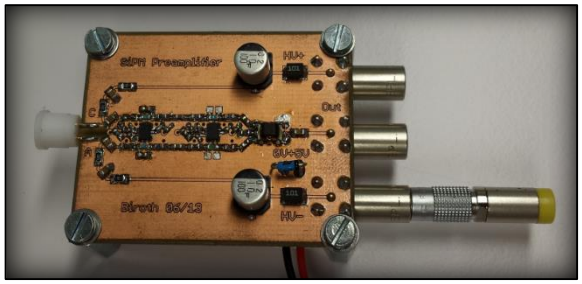
>>> ongoing development throughout 2013/14 <<<

Characterisation of SiPMs

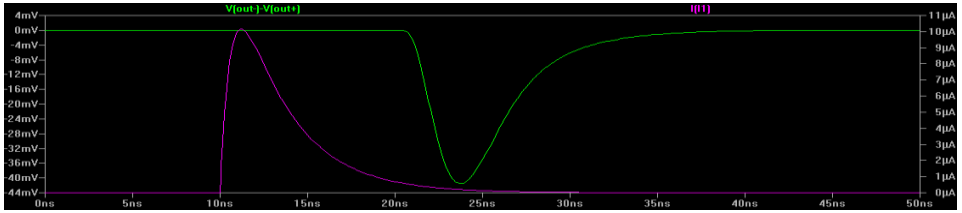
Explore properties of analogue SiPMs
- Signal shapes
  - After pulses
  - Cross talk
- Dark rates
- Absolute gain calibration
- Uniformity in sensitivity, gain and cross talk
- Thermal properties

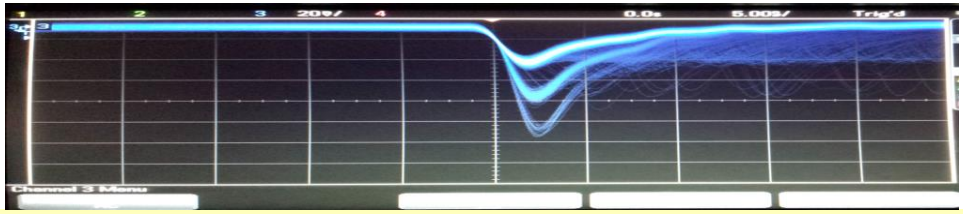


Require
- Readout chain for charge measurement
- Pre-Amp (provided by KPH)
- Pulse shape determination with FADC
- Pulsed laser diodes
- Optical table, positioning stage / stepper control
- Absolute charge measurements via pico-amp current readout (Xe-Lamp / monochromator, calibrated reference diode)



Status
- First simple readout chain working
- Simulating signal response
- Working on fast calibration pulser design
- Components procurement on-going





<<< Activities throughout 2013/14 >>>