Clock module (and other hardware)
- questions rather than answers -

post Palaiseau / pre DESY

nach dem meeting ist vor dem meeting

Mainz CCC saga, so far…

- no requirements known → no specifications written
  - „improve reliability, connectivity, jitter, and logic resources“
- Current CCC schematics available from the Web
  - Reverse-engineer the CCC (A.W.+R.D.)
  - Put “all” active components into single FPGA

  → Xilinx evaluation board (V6/7) + FMC daughter(s)
- Reinhold & Andre working on initial scheme/layout

Open questions :

- What active components **cannot** be moved into FPGA (level translators, comparators…) ?
- Protection of FPGA signal lines (2.5V maximum…) ?

CCC vs. TLU

30.11.11: phone call D. Cussans

- Build an „AIDA style TLU“, followed by a simple fan-out, i.e. trigger replicator is distinct from trigger generator
- Do the h/w in Mainz
- TLU-cum-CCC is FMC daughter
- Use reprogrammed DCC for fan-out (not finally agreed)
- Understand what asynchronous vs. synchronous trigger means for designers and consumers of clock unit
- Non-existent TLU design is non-documented at http://www.ohwr.org/projects/fmc-mtlu/wiki (will improve)
- Preferably CERN Cadence libraries to be used for common design(s) – trying to get access to CERN repositories

- Hope for some s/w & f/w support from Bristol (how realistic ?)

Some issues...

- Either have to rely on LAPP for providing and programming DCCs (Spartan-3?)
- Or MZ build both the clock and the fan-out module with FMC connectors to hook up on Xilinx ML605
- Or Mainz provide hard wired fan-out board
  - Understand fan-out/busy scheme and AC coupling (bias might be different for asynchronous trigger line, A.W./R.D.)
  - Long-term plans (Palaiseau meeting) are assuming crate based rather than table-top installations. Could be 1st candidate. 6U-VME format ?
- Fully synchronous processing **strongly** recommended for FPGA based designs
- Synchronous triggering requires additional TDC firmware on all asynchronous inputs (machine interface), plus readout of measured TDC values…
- If compatibility to asynchronous triggers were required there would be quite some bias towards a design that is *not* fully FPGA based (discrete replicators at least for the trigger line)

Before / at DESY meeting

- Come to a conclusion what **we** want and talk to David again
- Try to get more information on Kintex-7 board (connectivity!), assuming that we'd rather **not** buy additional V6 hardware
- Finalise (any) one suggested scheme/layout
- Will most likely never be built as designed
- Get prepared for discussions on synchronous trigger
- Prepare slides on clock module development and future LDA ! Who will go / who will present ?

- Collect input for
  - Number of HDMI fan-out channels
  - Jitter
  - Form factor

next:
- Reinhold status clock module
- Bruno drawing LDA++
- ???

And the final solution to it all:

Dear Uli Schaefer,

The Microelectronics Support Centre is pleased to announce that it has finalised an agreement with Calypto for the supply of Catapult via EUROPRACTICE.

Catapult High Level Synthesis reduces design time and verification effort by allowing hardware designers to use pure, untimed C/C++ for ASIC and FPGA design entry. No timing or architectural information is required in the C++ source, but is instead automatically added during the Catapult C synthesis process. This allows designers to quickly evaluate different architectures for given performance/area requirement without modification to the C++ source code.

→ The only missing link in the tool chain is the PowerPoint-to-C++ converter !!!!!!!!!!