The ATLAS Global Trigger Processor

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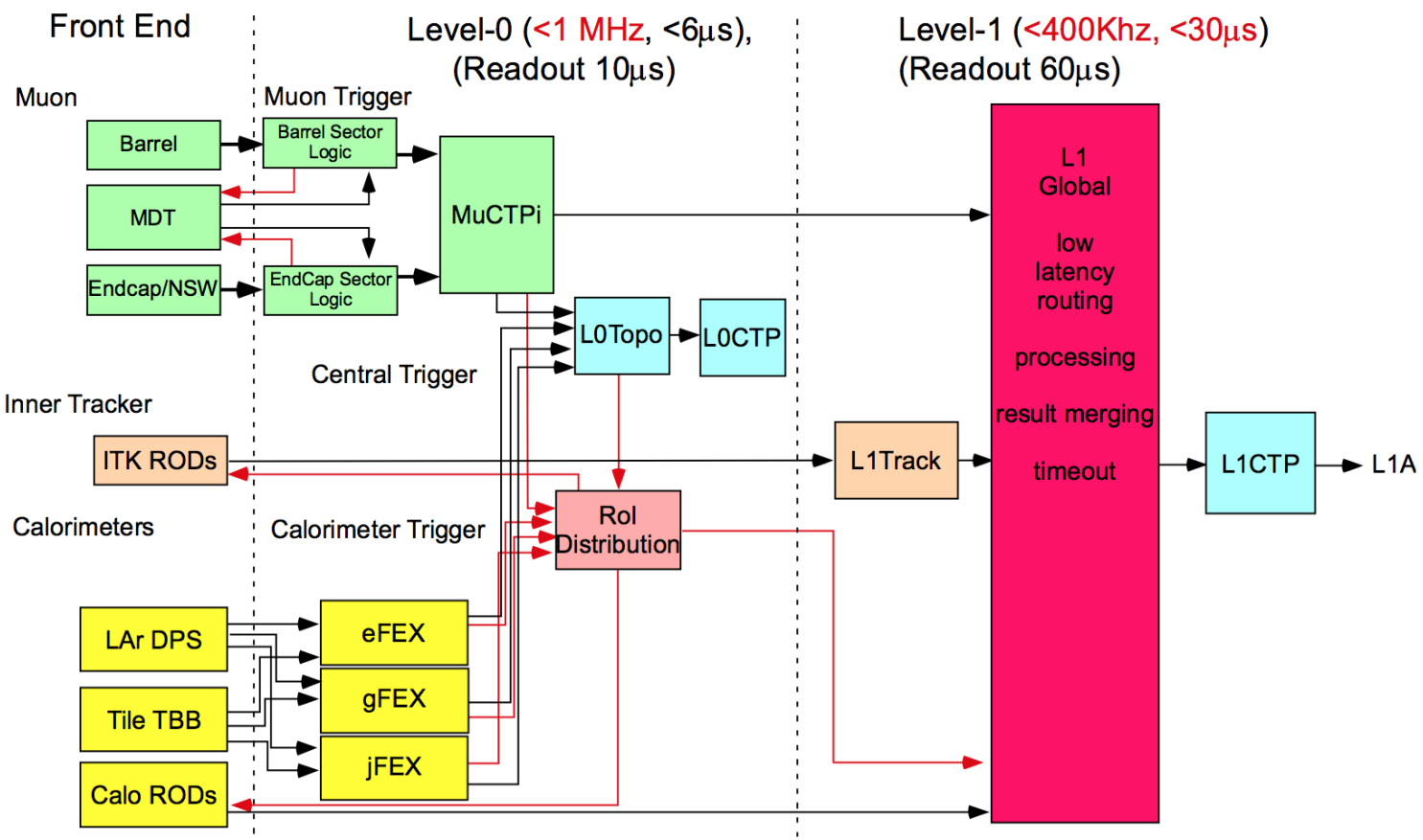
Phase-2 Upgrade

ATLAS Trigger upgrade Phase-2



- Re-baptise current Level-1 trigger (Calorimeters & Muons)
  → "Level-0" trigger
- Add track trigger
- **Add global level-1 processor**

Level-1 requirements

Currently (ATLAS Runs 1 & 2)

- Very low trigger latency (2.5µs) including cabling (!)
- Fixed latency, pipelined processor
- Dead time-less system
- Operating at 40,08 MHz LHC bunch clock or multiples

→ Processors based on ASICs and FPGAs only

Separate feature extraction stage for various trigger object types

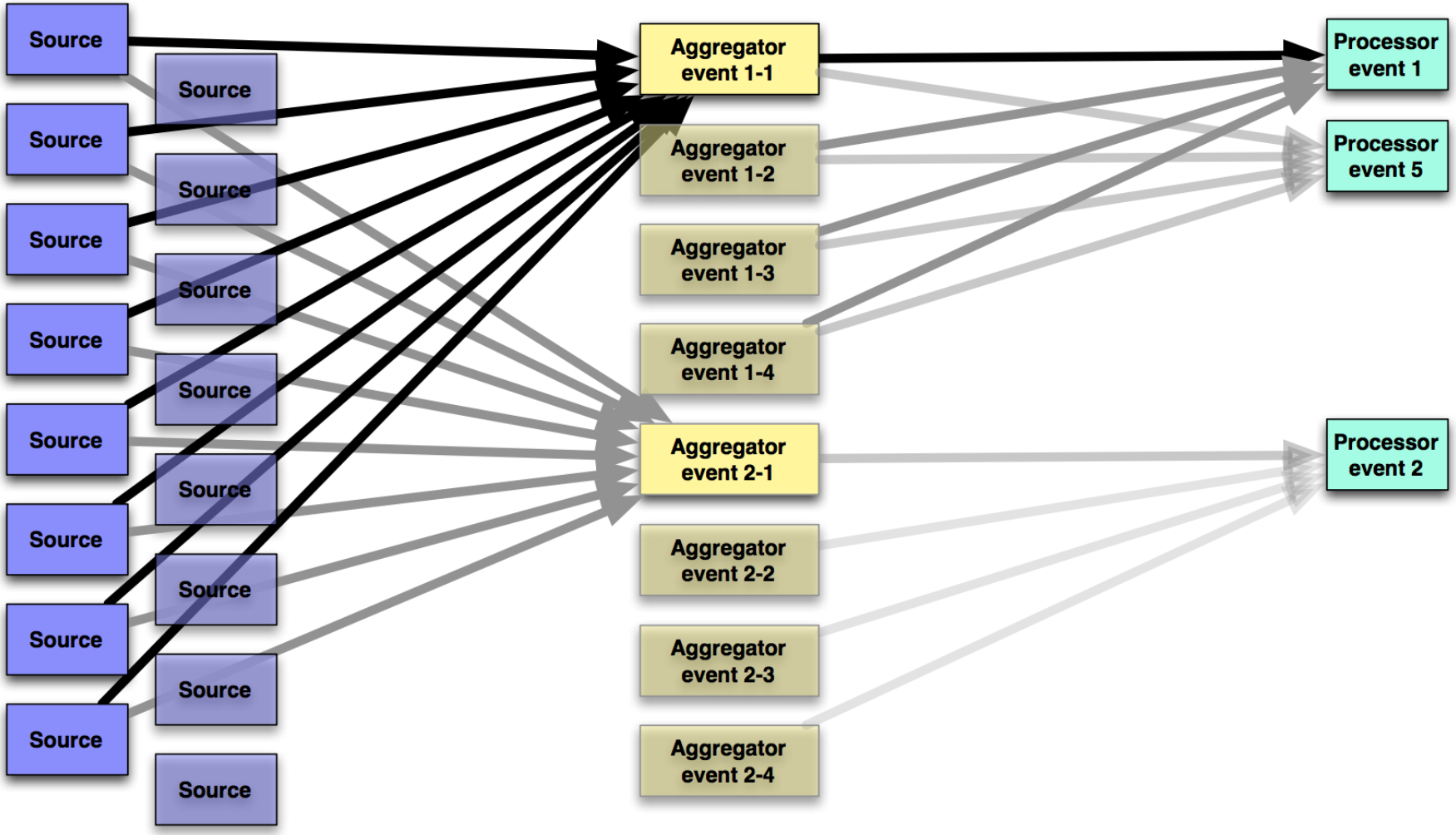
Post upgrade

- Low latency (x10)
- Some de-randomizing possible, but still limited latency
- Very low dead time is acceptable
- Not necessarily tied to LHC bunch clock

→ any alternatives to FPGA based scheme ?

Process all trigger objects in one processor (per event) to correlate them

ATLAS Global Level-1 Processor



Latency: spend on processing, not on routing / buffering !!!!

Activities -- L1Calo Mainz / PRISMA

- Initially: **architectural** discussions
  - First conceptual design under way
  - FPGA based
  - A couple of feeder FPGAs
  - Powerful processor FPGA
- Thorough module level planning / **Simulation**
  - Power
  - Thermal (!)
  - Signal integrity
  - …
- **Evaluation** of high-end processors available on the markets
  - Link bandwidth
  - Link count
  - Processing power
  - **Xilinx**, **Altera**, … ???... ??? / Eval boards ?
- **Demonstrator** module
  - Detailed design from mid 2016
  - …