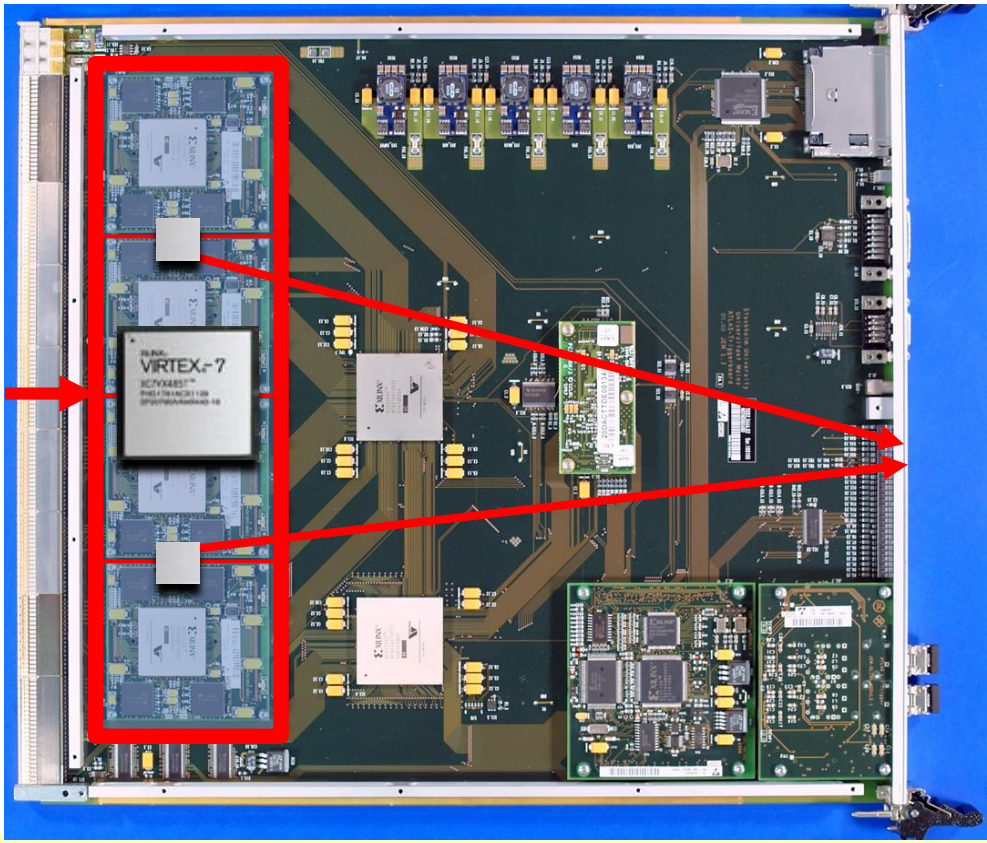
JEM Mezzanines – the details

Currently four input modules per JEM

- 88*10-bit input from four PreProcessors total
- 32 electromagnetic and 32 hadronic core channels plus environment

Replace with single module

- Early replacement in case of excessive failures of current daughters
- Otherwise in time for phase-1
- Rigid / flex PCB
- Single large Virtex FPGA to support required connectivity
- Receive 960 Mb/s electrically
- Loop through to MGTs w/o processing
- Run through MicroPOD opto-transmitters
- 5 fibres worth of incoming tile data at 6.4 Gb/s baseline
- 4 copies to FEXes via front panel (MPO/MTP)
- Replacement required on all JEMs (32 plus spares)



Cost and effort

- Small module, 40-off production
  - **If pre-phase 1 functionality is to be kept alive**, large FPGA is required
  - FPGA dominates cost at ~7,500€/chip
  - Per-module cost well below 10k€
  - Discarding pre-phase 1 functionality will allow for mid range Kintex FPGA at < 5k€/module

- Effort required / available in Mainz :~1.5 FTE total sum for Kintex approach
- Another half FTE on firmware for integration with existent JEM functionality