Proposal for a versatile Readout for Scintillator Test Stands

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Why a Common Readout?

Typical test setup:

- Scintillator/fibre/PMT/SiPM/... shall be tested for light yield, time resolution, uniformity, etc.
- Light sources may be cosmics, LEDs, laser, or radioactive sources.
- Triggering usually done by 1 or 2 trigger scintillators + light guides + PMTs (or just by e.g. the LED trigger).



Common readout very useful for all different test setups

(Trigger for this proposal: Test measurements for CALICE, NA62 Muon Veto, and NA62 Hodoscope)

Requirements for a common Readout System

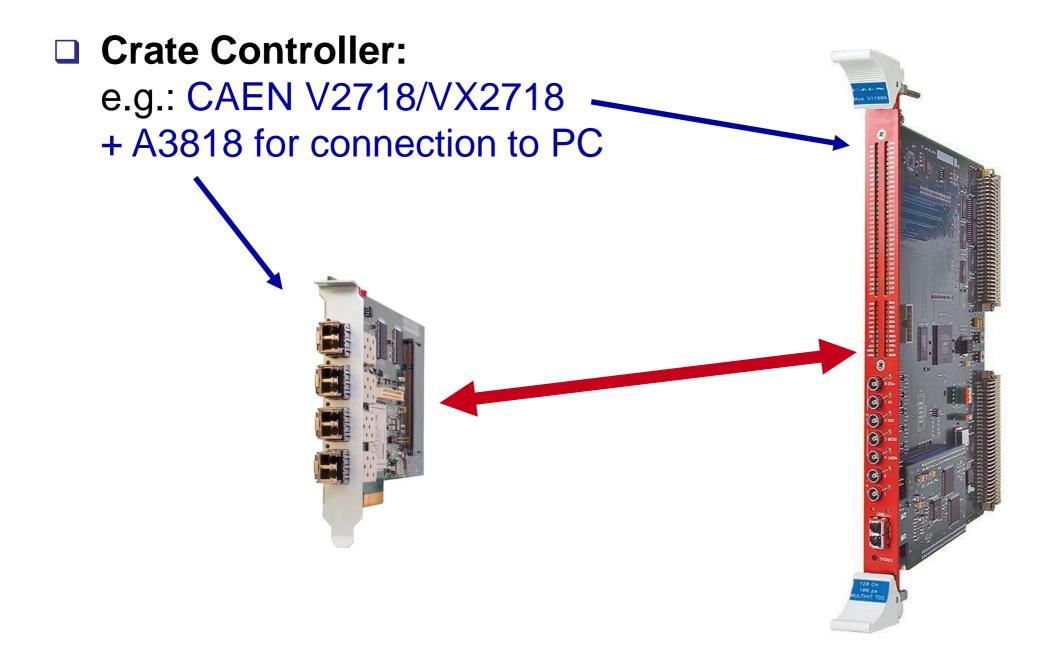
Wish list for a common multi-purpose readout system:

- □ Charge, amplitude, and time resolution as good as possible to be suitable for all different applications. $(\sigma_Q \sim 0.1 \text{ pC}, \ge 10 \text{ bit ADC}, \sigma_t \ll 1 \text{ ns for pulse widths of } \mathcal{O}(10 \text{ ns}))$
- Discriminators, coincidence units, fan-out, amplifier, etc. for triggers and multi-purpose use.
- □ "Plug & play" for fast and simple use.
- Software should be reusable, but also easy to expand for nonexperts.
- □ **Mobility** for use of different test stands.

Requirements for a common Readout System Pulse midth (2(10ns) . (rate + PS Time resolution ~ 0.1-0.2ns · Change. QDC/FADL 5 ~ O.N PC L' FADL simplify in Timing . TDC/FADL OF & 1 ns 3 1 GHZ - Amplitude: ADC/FADL > 12 bits Channels: 8-10 . Frequency: Scaler Discriminators/Gincidence 4/ UMDr Analog Fan-Out, Amplifier, Conholled by VME FADC + QDC/TDC/ Philse Consultor, Times UME CPU Cables 100 Lanua (100 Ba

Modules

One common VME crate, controlled by a CPU or similar with (possibly) a multi-channel FADC or digitizer and other modules for amplification, discrimination, coincidence, etc.



Modules

FADC/ADC: e.g.: Struck SIS 3305 10-bit FADC or CAEN V1742 digitizer



- Single width 6U VME card
- 2/4/8 channels
- 5 GS/s/2.5 GS/s/1.25 GS/s per channel
- 512/256/128 MSamples/channel memory
- 2 GHz bandwidth
- Internal/External clock
- readout in parallel to acquisition
- Multi event mode
- Sparsification
- Pre/Post trigger capability
- Trigger or output (4 individual thresholds)
- A32/D32/BLT32/MBLT64/2eVME/SST
- 1/2/4 GBit/s optical link option
- In field JTAG and VME firmware upgrade capability

(also in use by Xenon group)



- 0 32+2 channel
- 12 bit; Selectable 5, 2.5, 1 GS/s Switched Capacitor ADC
- 1 Vpp input dynamics, single ended, 50 Ohm, MCX coasial connectors
- Based on DRS4 chip (Paul Schemer Institute design)
- 1024 storage cells per channel (200 ns recorded time per event (§ 5GSample/s)
- Trigger Time stamps
- Memory buffer: 128 events/ch (optional: 1024 events/ch)
- Dead Time: 110µs Analog inputs only, 181µs Analog inputs + TR0, TR1 inputs
- Possibility of FPGA for real-time data processing (for example Zero Suppression and Data Reduction algorithms)
- VME64X-compliant and Optical Link Interfaces
- PCI controller available for handling up to 8 Modules daisy chained via Optical Link
- Firmware upgradeable via VME/Optical Link.
- Libraries (C and LabView), Demos and Software tools for Windows and Linux

Very rough Cost Estimate

VME 64x standard Crate:	7 k€

- □ VME master module/CPU: 5 k€
- □ 10-bit FADC or equivalent: 14 k€
- → In total: ~ 26 k€

Other VME-controlled modules (trigger logic, discriminator, ...): ~ 2 – 3 k€ each

Decision on specific modules to be taken after discussion with all participating groups (and solid offers, of course).

... extend for upcoming R&D

- Large scale experiments (most CERN experiments including ATLAS) moving on to xTCA shelf architecture
- First ATCA based R&D projects imminent
- Complement the "classic"
 VME based systems by
 ATCA equipment

ATCA shelf incl. shelf manager and power supplies ~ 10k€



Further needs (general use)

For any kind of lab we require

- Oscilloscope (1.5GHz + probes) 20 k€
- Pulse generator ~5 k€
- Meters...

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k€