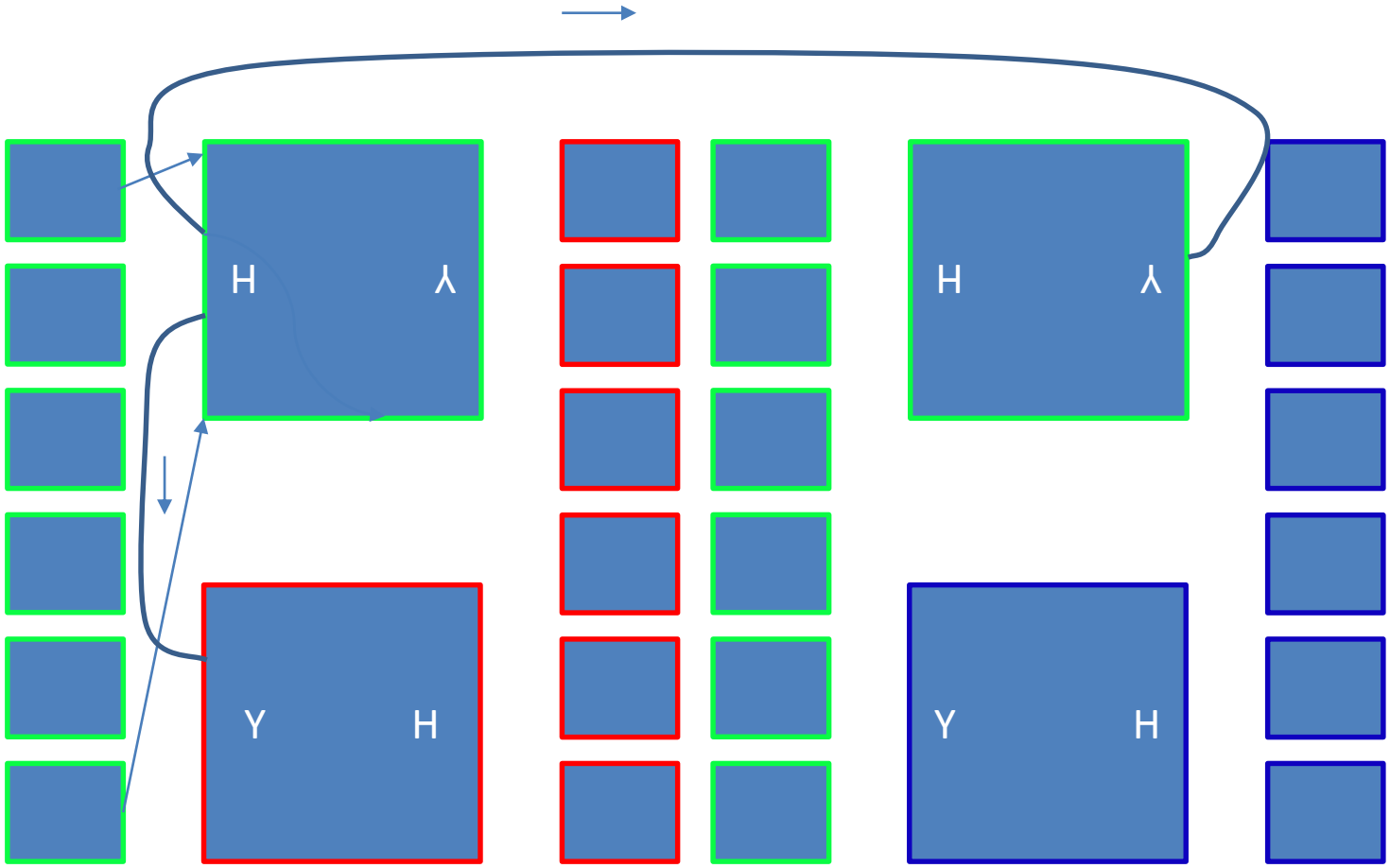

Boxes to scale. Distances not to scale (routing channels !)

Placement / routing option 1

- **Route MGT links once and copy for all four instances**
- Breakout and routing (layer use) similar to Topo
- mPOD breakout on sig1, capacitors close to mPOD, from there stay on top and route into MGTH inputs on top layer
- Breakout of GTH TX (loopback) on sig1, near GTY TX go to top layer and mount capacitors there (if required)
- 5 mPODs required for input purposes. 6th mPOD is actually available for output signals.

Unresolved so far:

- sig1 routing area of mPODs needs to be kept away from sig1 routing of loopback signals. That might require spreading out the design horizontally. Loopback routing channel needs to be ~25mm (30 lanes each way)
- On L1Topo we have minor impedance discontinuities on top layer just before RX pins. Can we minimize that ?
- TBD: shown layout nicely separates rows belonging to FPGAs. That will, however make some traces longer…
- We have not yet any routing scheme for the (few) output links. Possible: break out on sig1, route to top before crossing the loopback channel and pass over it on top…