LVDS Source Module. (LSM)

LVDS source module for 480Mb/s serial data. For testing CPM and JEM processor modules .

As with the DSS, but driving many more links, the LSM would use FPGA data generators feeding LVDS serialisers driving cable connectors.

TTCdec module will provide the clock, and have electrical and possible optical TTC inputs. There will also be an onboard xtal oscillator for testing. These will feed the PLL clock distribution.

FPGA configuration will be held in FLASH memory.

A DC/DC converter will provide the onboard 3.3V supply.

JTAG connections will be used for assembly testing.

However , there are still some decisions to be made:

Module size.

6U VME preferred. 9U may have assembly issues.

Pattern Generator Memory depth.

≤ 4k depth can be provided within chosen FPGA,
(Xilinx XC2v250) possibly allowing 88 links / LSM.
Larger FPGAs available, but at far greater cost.

> 8k depth requires memory external to FPGA,
If BGA packages are used for the memory then 32 or even 48 links per LSM are possible. Current consumption estimated at 3.3A and 5.1A respectfully.(see below) 128k depth are standard.

LVDS serialisers

The Octal LVDS serialisers are more compact but do not have JTAG/BS functions and their drive current is less than that of the single parts. Virtex2 could serialise , but this is untested.

Cable drivers + Cable Pre-compensation

Existing DSS/LVDS has 8mA Current drivers with LR pre-compensation across line.

Pre-processor will possibly use Virtex FPGA outputs which are really voltage drivers. What is the compensation circuit?

Cable connectors.

These will be compatible with our miniature cable assemblies. The intended connector as used on the new DSS/LVDS is 17mm wide and overhangs the adjacent slot by 1.5mm.

Signal layout should match that of the processor backplane, with its 6 cable connectors (5 used by CPM , 5½ used by JEM).

1 LSM = 1 JEM/CPM , 88 links / LSM

If we cant fit 88 links onto LSM , then how many links / LSM ?
1 connector = 16 links.

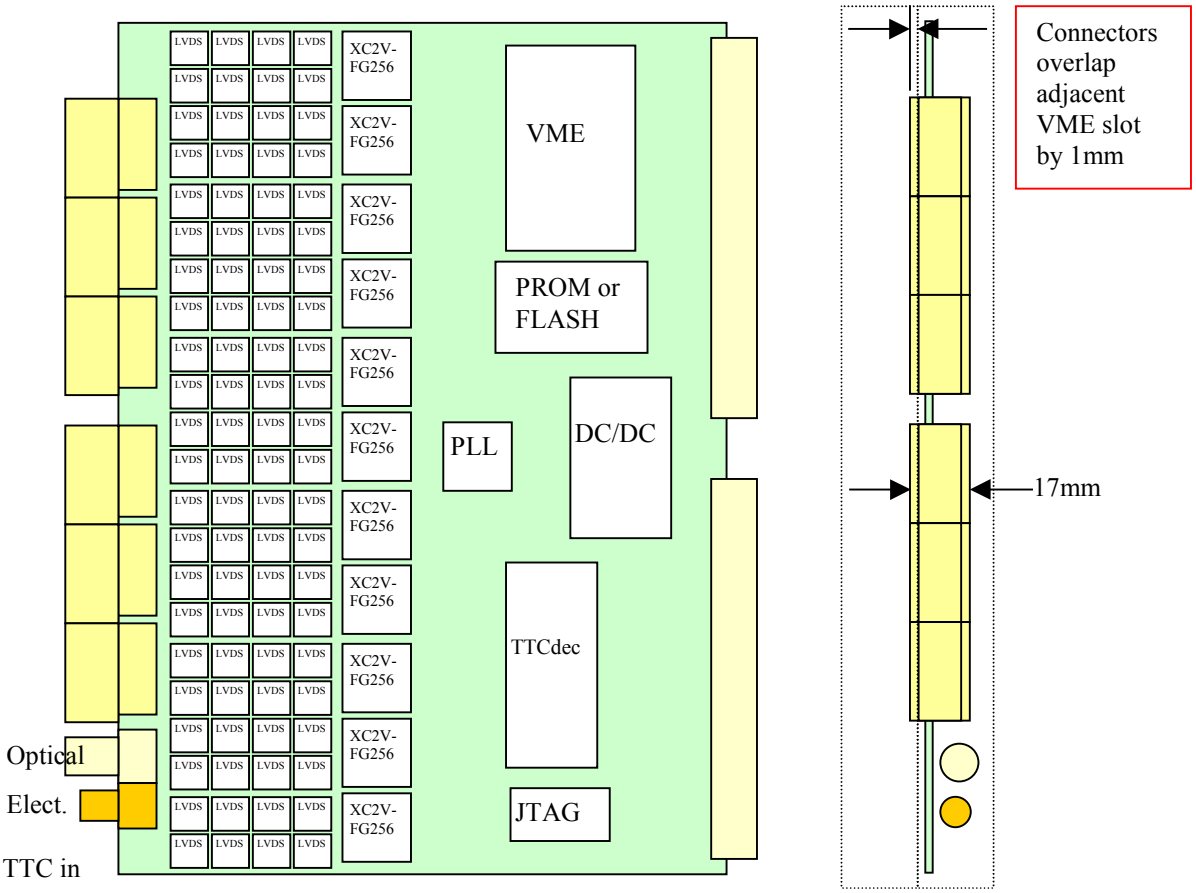
2 LSMs = 1 JEM/CPM	3 connectors - 48 links
3 LSMs = 1 JEM/CPM	2 connectors - 32 links
4 LSMs = 1 JEM/CPM	3 'half connectors' - 24 links

The two diagrams on following pages show the module after certain choices have been made:

A 'baseline' design:

FPGA using internal memory +
JTAG LVDS (SCAN921023)

88 links each with 4k deep pattern memory



Side view

Front view

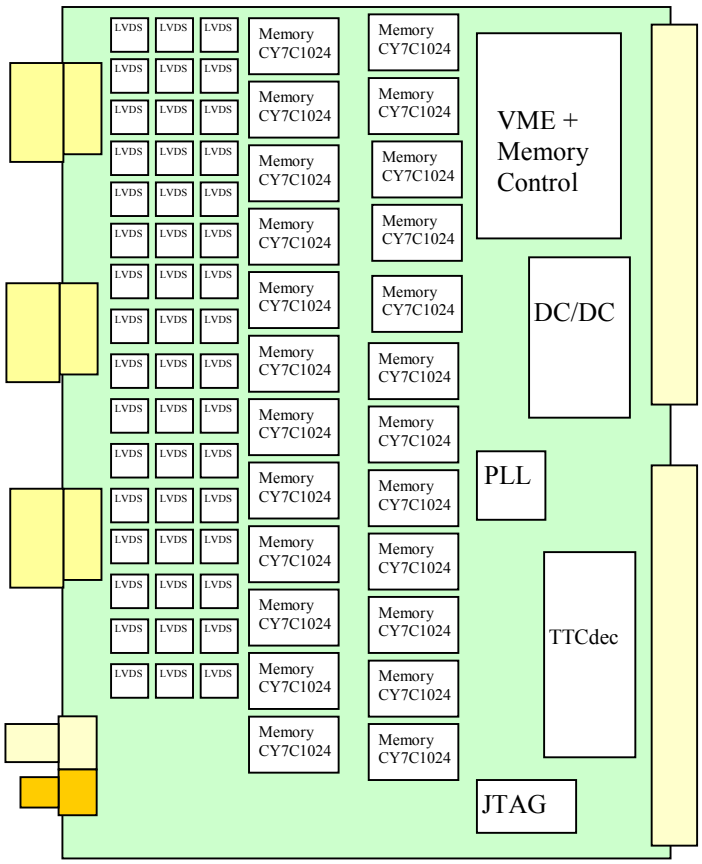
Current consumption at 3.3V.
88 LVDS serialisers @40MHz, Total = 4.2 A.
FPGA consumption ?

Estimated Component Cost excluding connectors: 1200 EUR

Discrete LVDS design:

FPGA with external memory +
JTAG LVDS (SCAN921023)

48 links each with 128k deep memory (in BGA package)
(CY7C1024 128K x 24 in BGA)



Current consumption at 3.3V

48 LVDS @ 45mA	= 2.2A
24 memories @ 120mA	= 2.9A
Total	5.1A

Further ideas can be found at:

http://www.ep.ph.bham.ac.uk/user/staley/LSM/

R.Staley 05 March 2003